



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 035905/0104

In re patent application of

Thomas H. LEE et al.

Serial No. 09/927,648

Art Unit: 2818

Filed: August 13, 2001

Examiner: Unassigned

For: DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND
METHODS FOR MAKING SAME

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the first Office Action on the merits, please amend the application
as follows:

In the Specification:

Please amend Page 1 of the specification by replacing the first paragraph after the
Title with the following paragraph:

This application is a continuation-in-part of U.S. Application Serial Number
09/801,233, filed on March 6, 2001, which is a continuation-in-part of U.S.
Application Serial Number 09/745,125, filed on December 21, 2000, both of
which are incorporated by reference in their entirety. This application is also a
continuation-in-part of U.S. Application Serial Number 09/639,579 filed on
August 14, 2000, which is incorporated by reference in its entirety. This
application is also a continuation-in-part of U.S. Application Serial Number
09/639,702 filed on August 14, 2000, which is incorporated by reference in its

entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,749 filed on August 17, 2000, which is incorporated by reference in its entirety. This application also claims benefit of priority of provisional application 60/279,855 filed on March 28, 2001, which is incorporated by reference in its entirety.

REFERENCE IN ITS COVER

Application 805518-222 filed on March 28, 2001, which is incorporated by

[illegible]

application 60/279,855 filed on March 28, 2001, which is incorporated by reference in its entirety.

entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,749 filed on August 17, 2000, which is incorporated by reference in its entirety. This application also claims benefit of priority of provisional application 60/279,855 filed on March 28, 2001, which is incorporated by reference in its entirety.

SCANNED, # 1

REMARKS

The Preliminary Amendment is submitted to correct the filing dates of two priority applications Serial Number 09/745,125 and 09/637,749 provided on page 1, paragraph 1 of the application, such that these filing dates correspond to the filing dates officially granted to these priority applications by the USPTO. The corrected filing dates of these two priority applications also correspond to the filing dates noted for these applications on the Filing Receipt mailed September 14, 2001.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

11/14/01
Date

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Reg. No. 4,445

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Fax: (202) 672-5399

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY DEFICIENCY OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 19-0741.

Redlined Version of the Amendment to Show Changes Made

This application is a continuation-in-part of U.S. Application Serial Number 09/801,233, filed on March 6, 2001, which is a continuation-in-part of U.S. Application Serial Number 09/745,125, filed on December 21 [22], 2000, both of which are incorporated by reference in their entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,579 filed on August 14, 2000, which is incorporated by reference in its entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,702 filed on August 14, 2000, which is incorporated by reference in its entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,749 filed on August 17 [14], 2000, which is incorporated by reference in its entirety. This application also claims benefit of priority of provisional application 60/279,855 filed on March 28, 2000 which is incorporated by reference in its entirety.

SCANNED, # 2

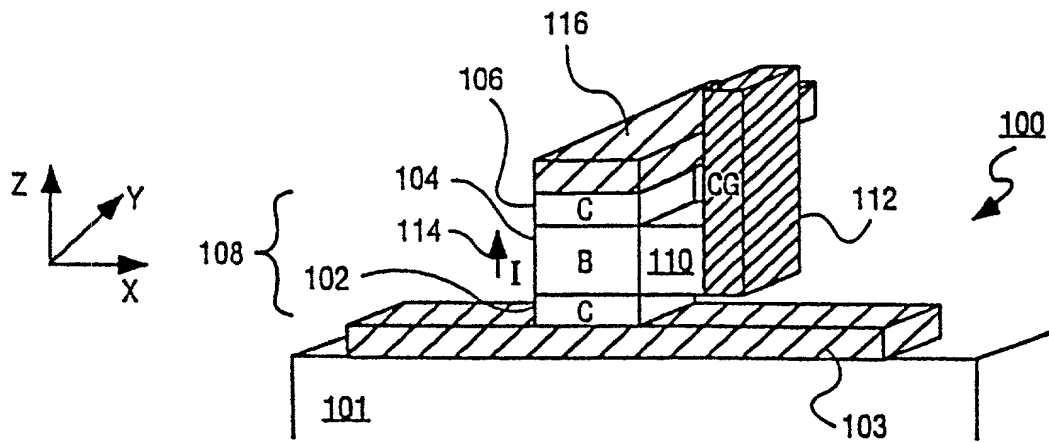


FIG. 1A

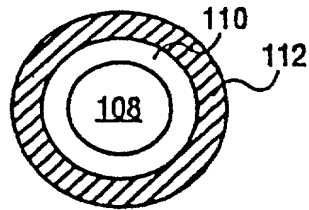


FIG. 1B

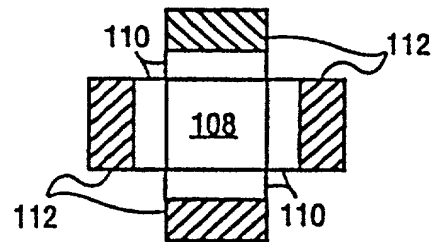


FIG. 1C

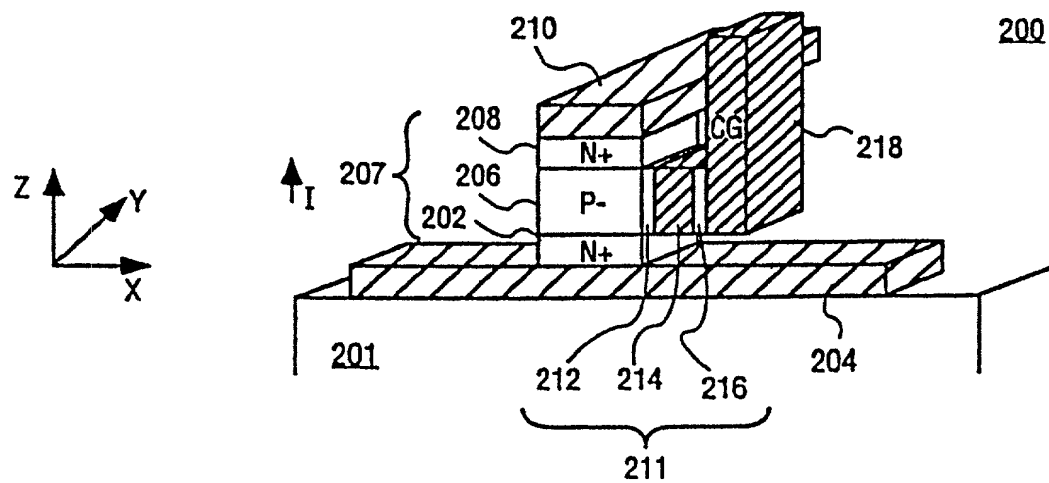
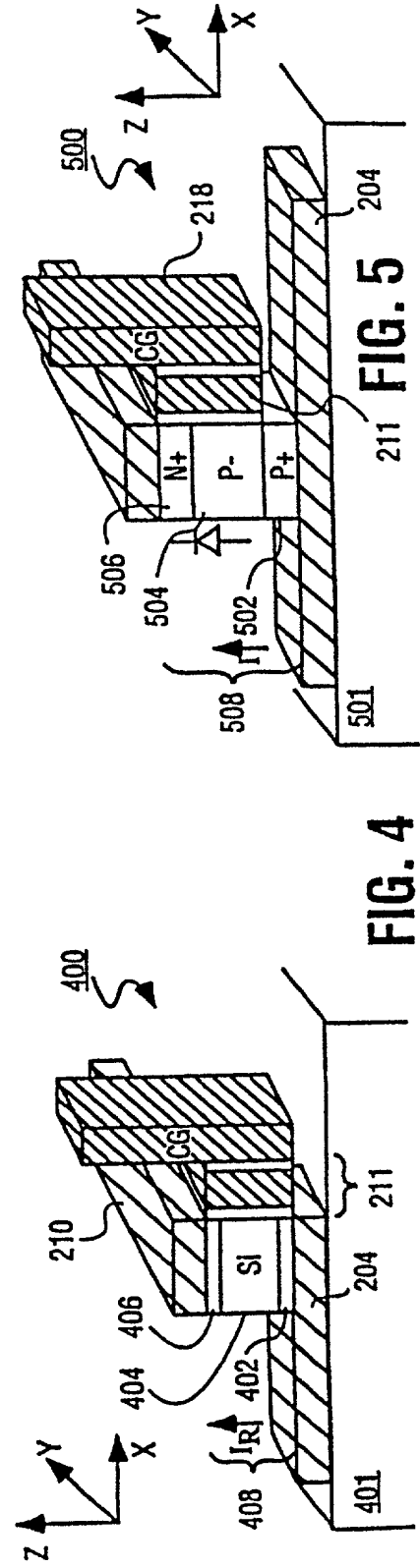
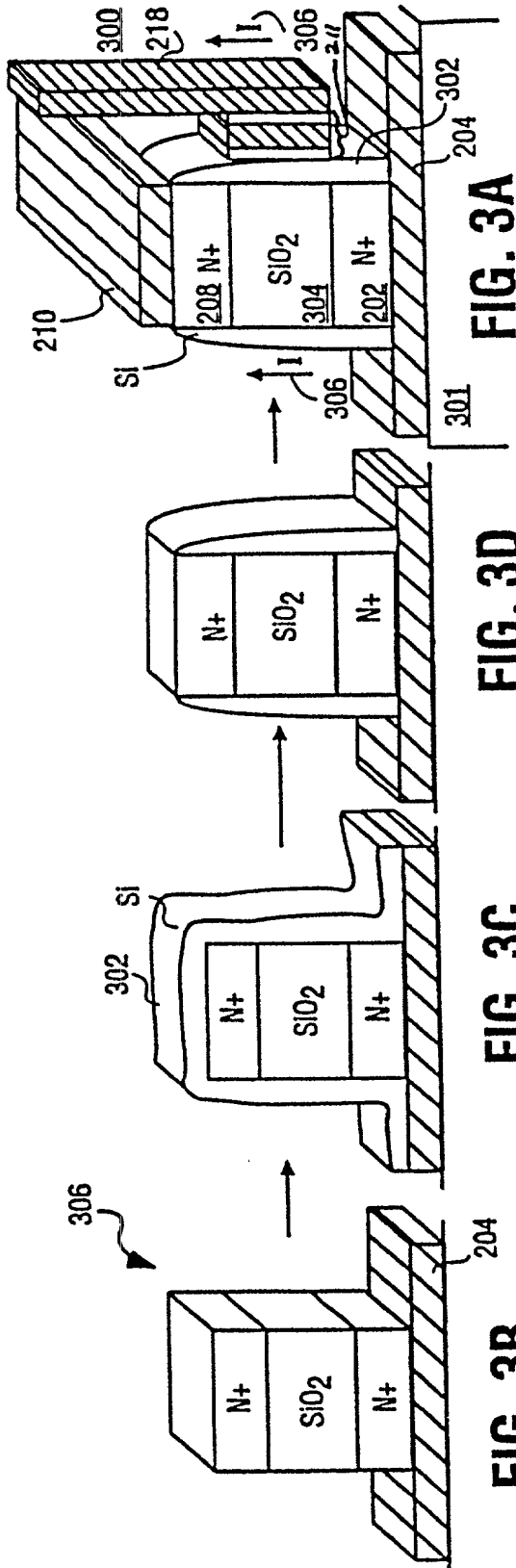


FIG. 2



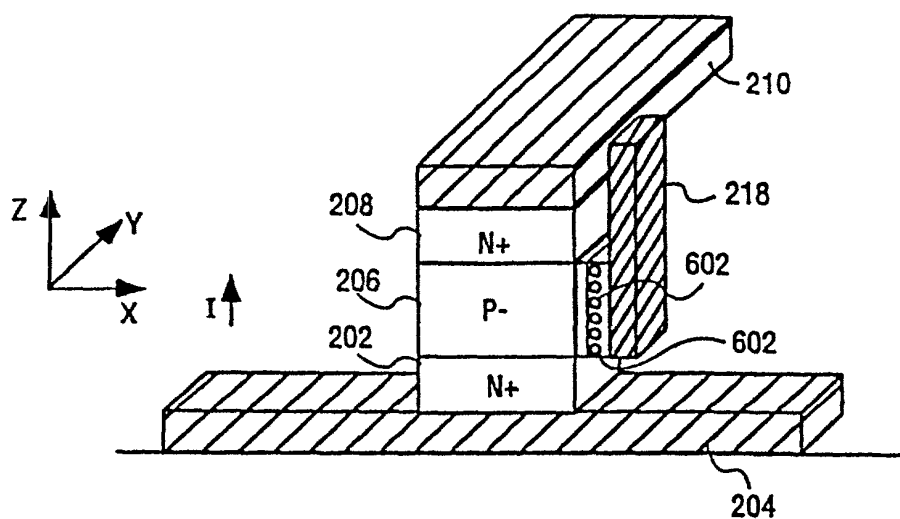


FIG. 6

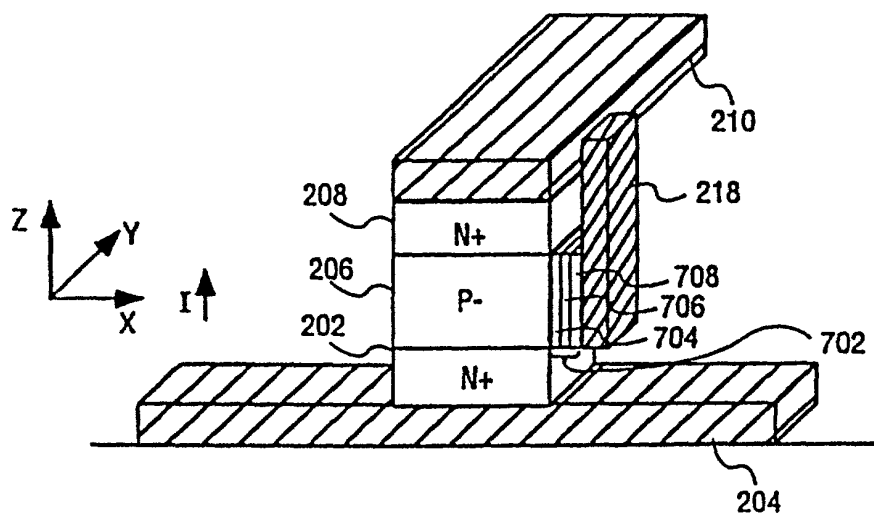


FIG. 7

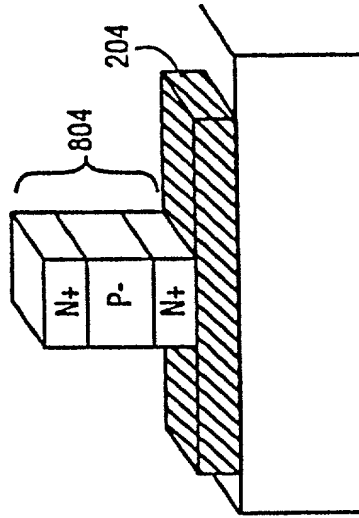


FIG. 8B

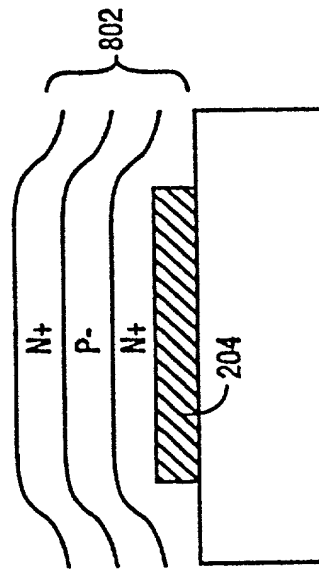


FIG. 8A

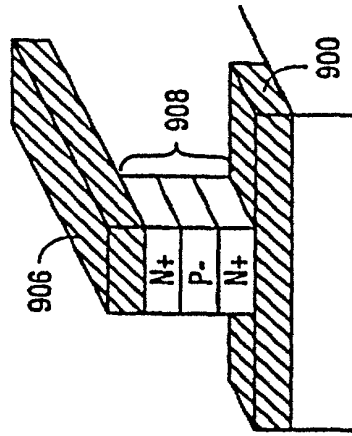


FIG. 9B

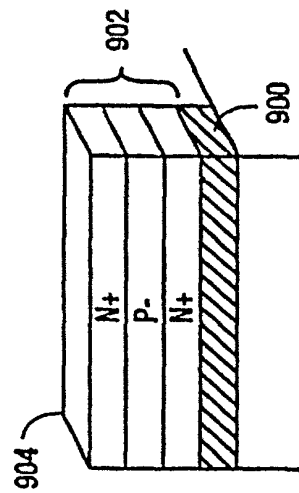


FIG. 9A

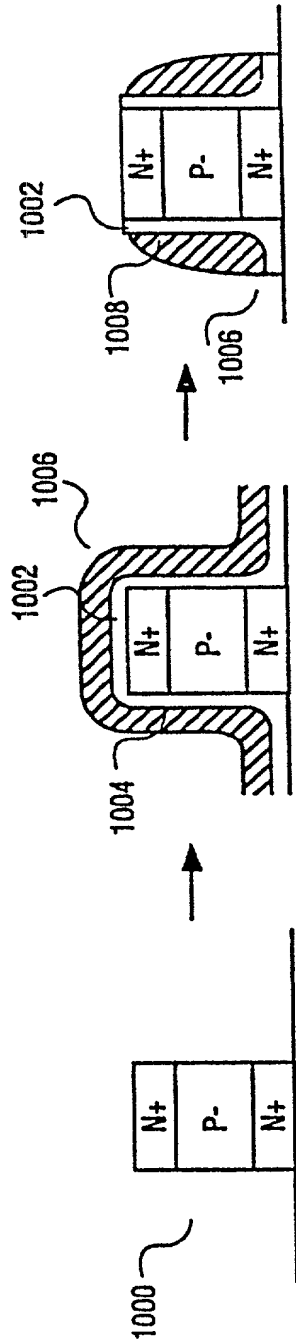


FIG. 10A

FIG. 10B

FIG. 10C

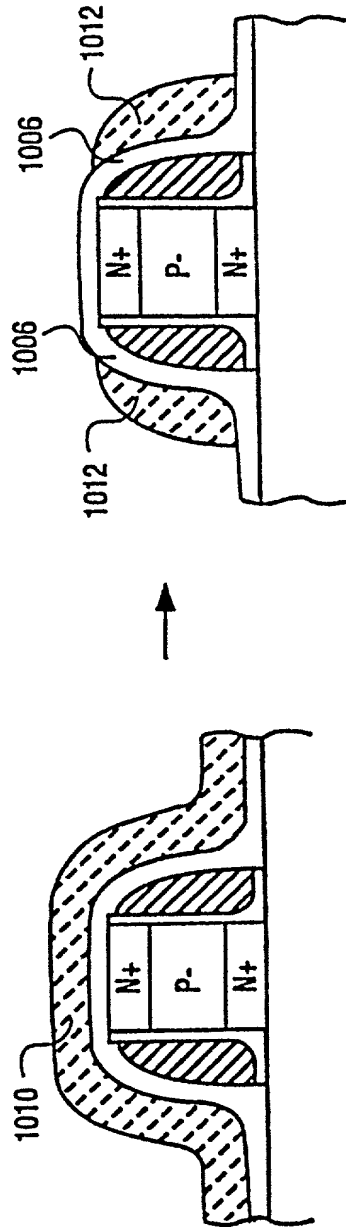


FIG. 10D

FIG. 10E

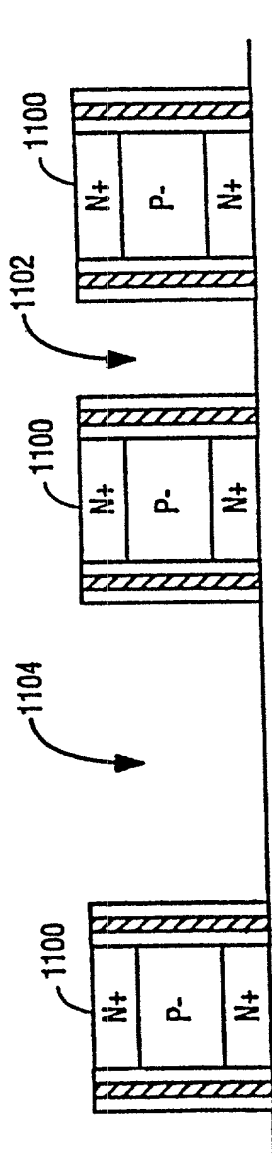


FIG. 11A

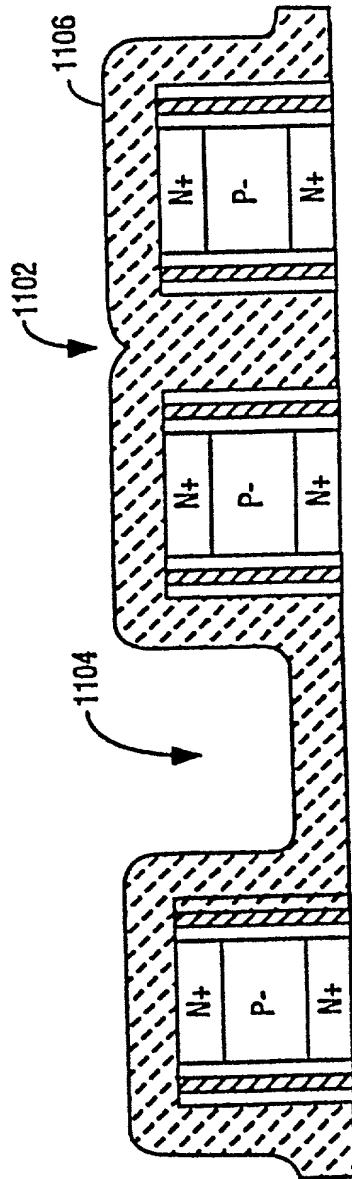


FIG. 11B

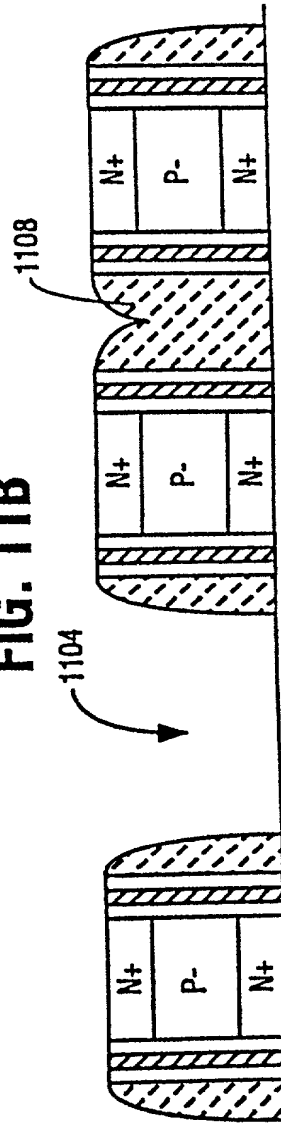


FIG. 11C

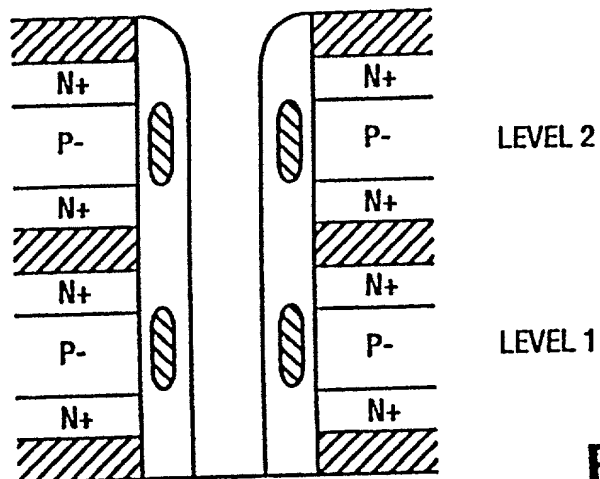


FIG. 12A

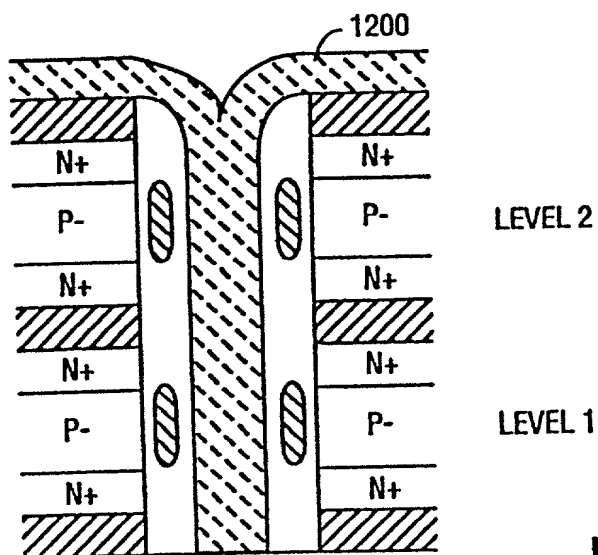


FIG. 12B

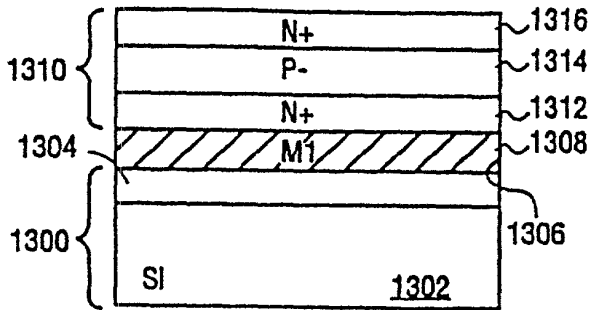


FIG. 13A

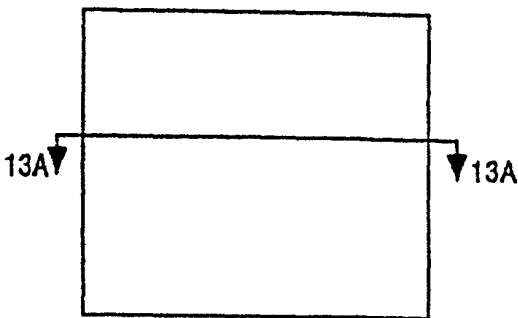


FIG. 13B

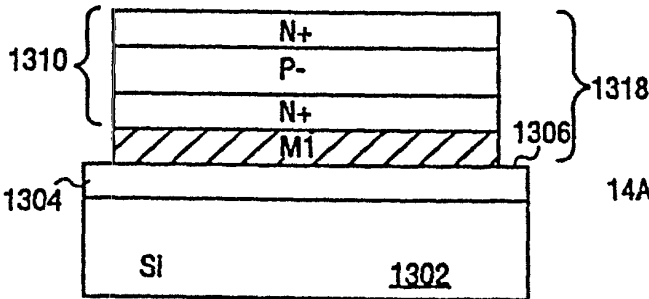


FIG. 14A

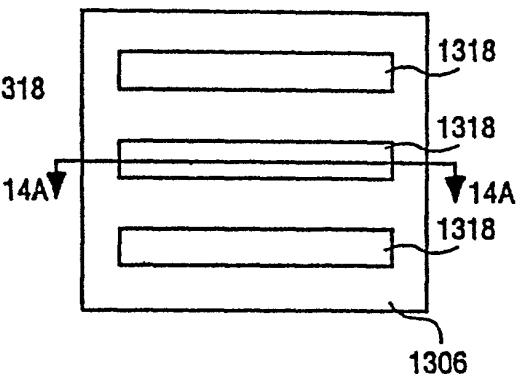


FIG. 14B

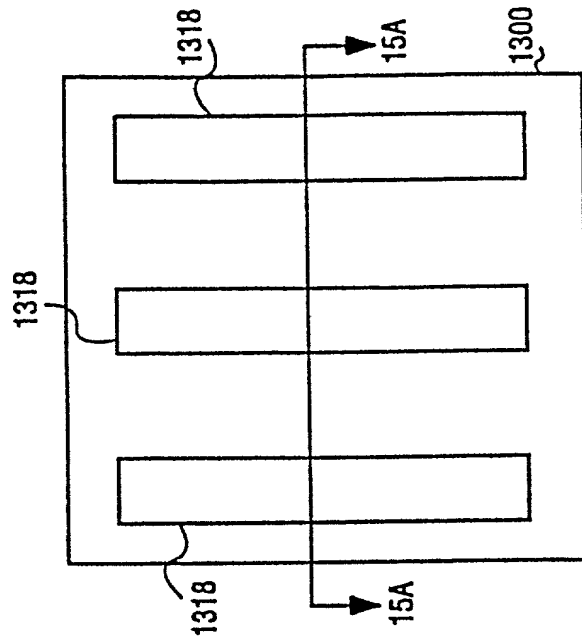


FIG. 15B

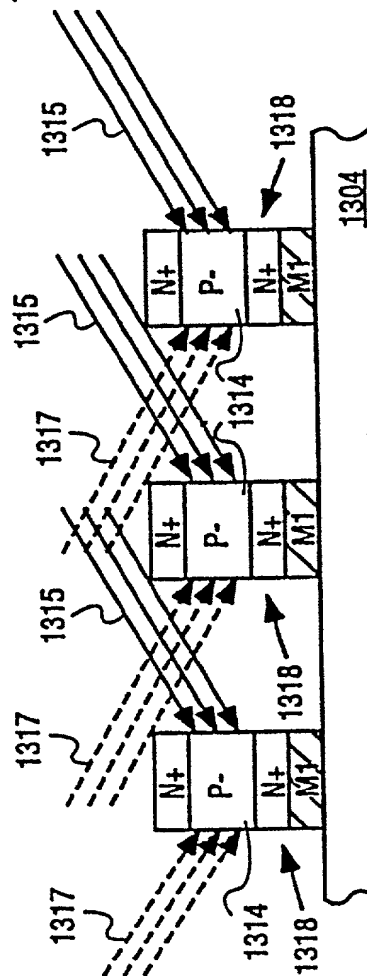


FIG. 15A

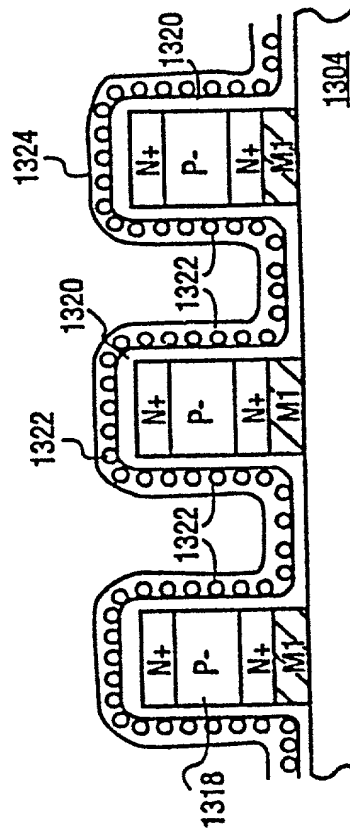
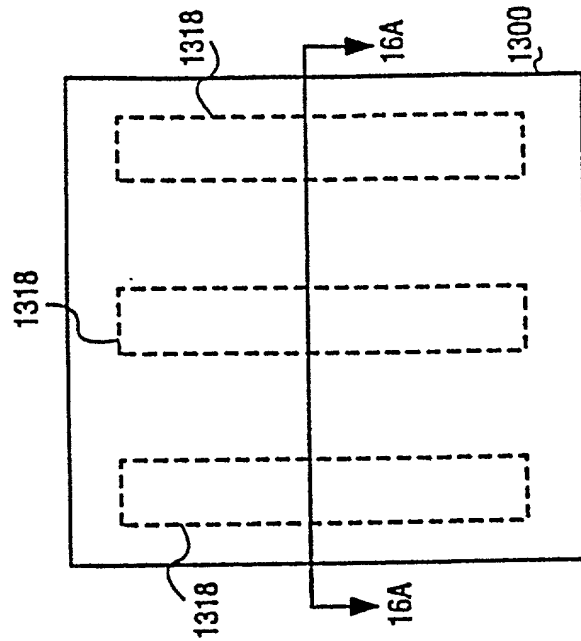


FIG. 17A

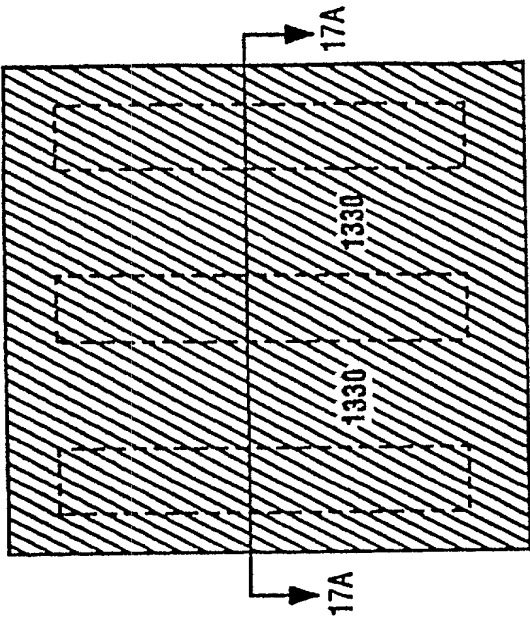


FIG. 17B

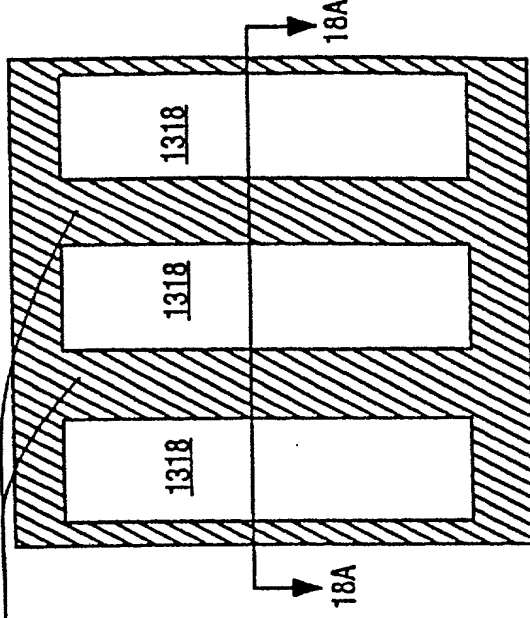


FIG. 18B

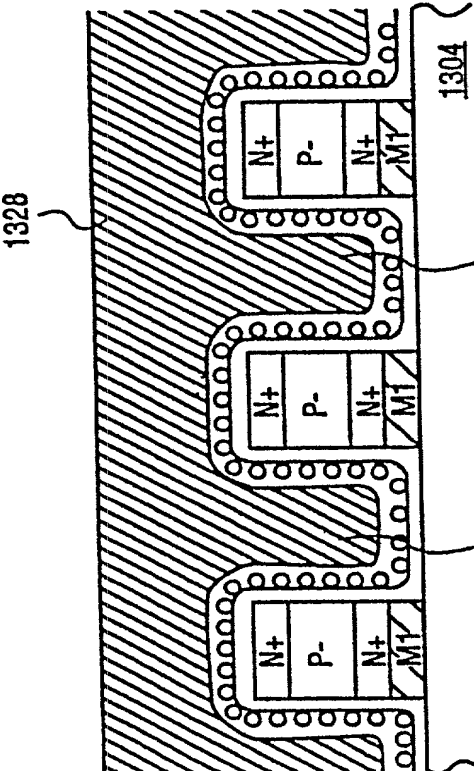


FIG. 17A

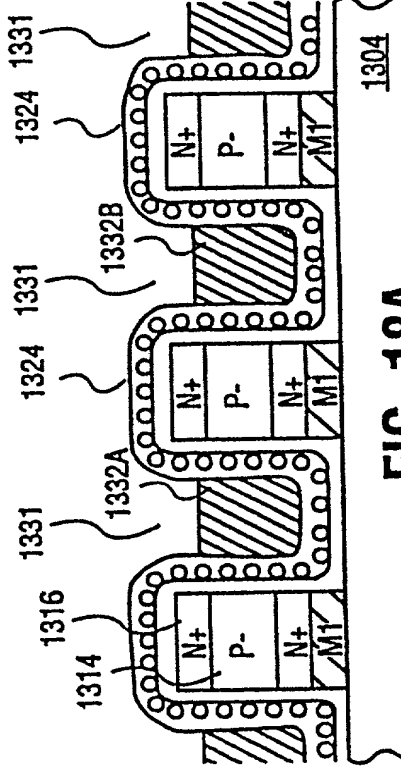


FIG. 18A

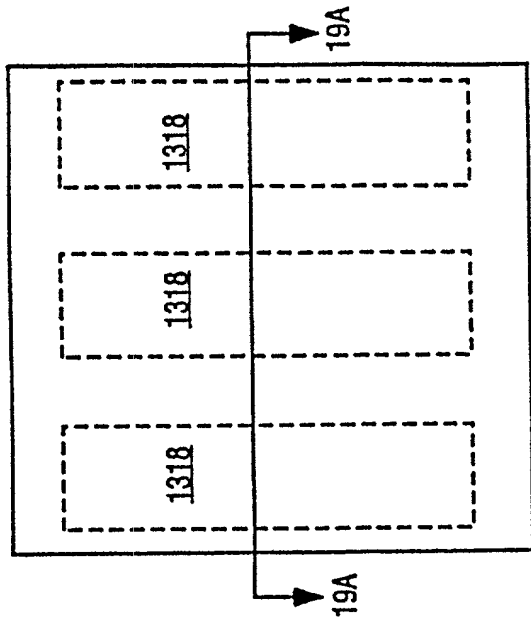


FIG. 19B

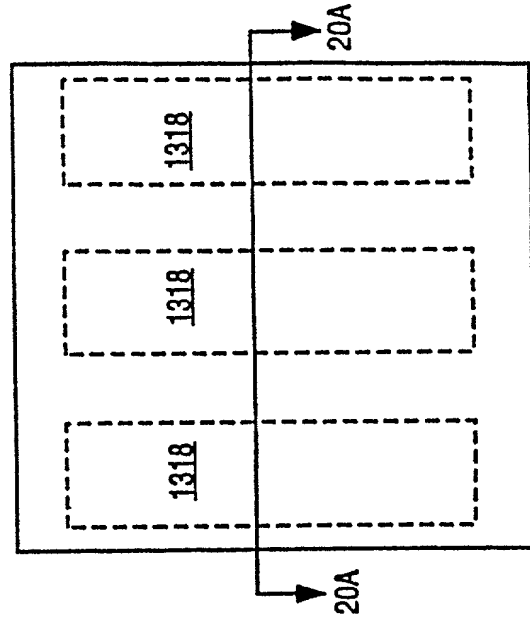


FIG. 20B

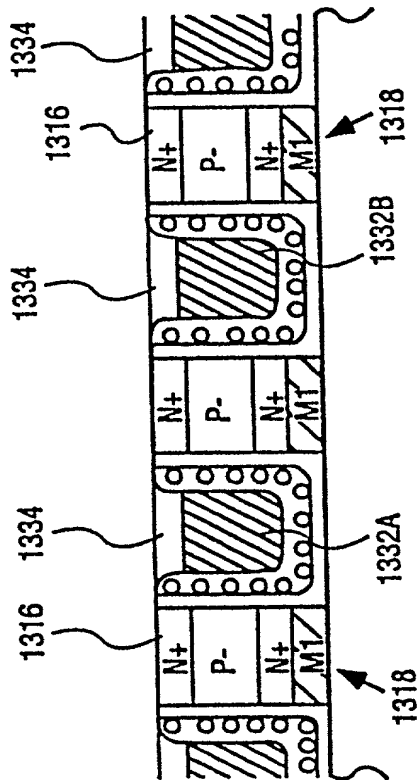


FIG. 19A

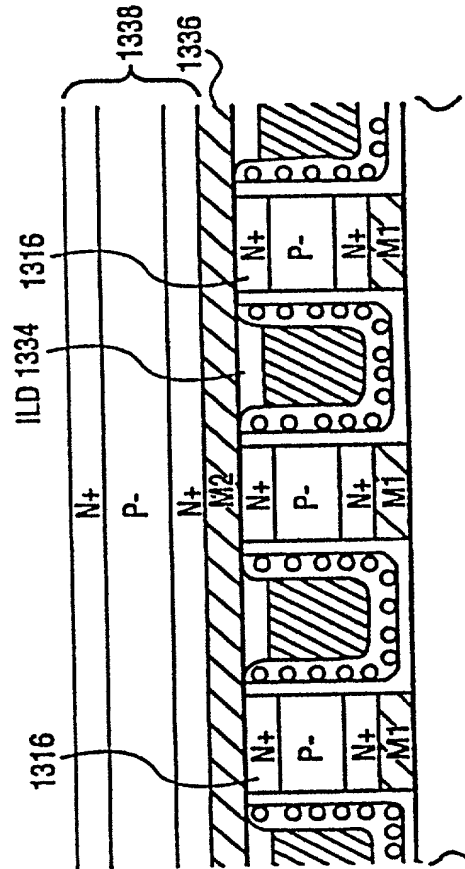


FIG. 20A

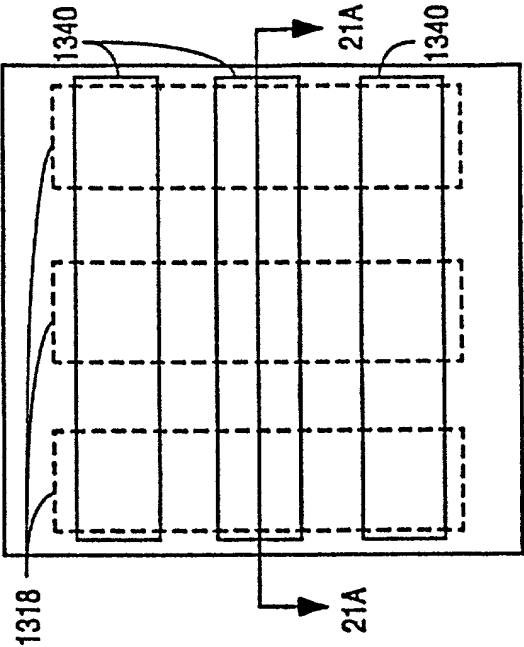


FIG. 21B

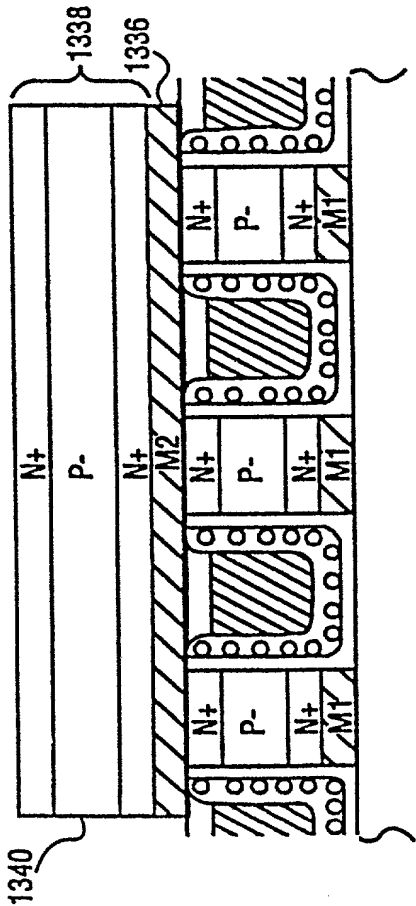


FIG. 21A

FIG. 21A

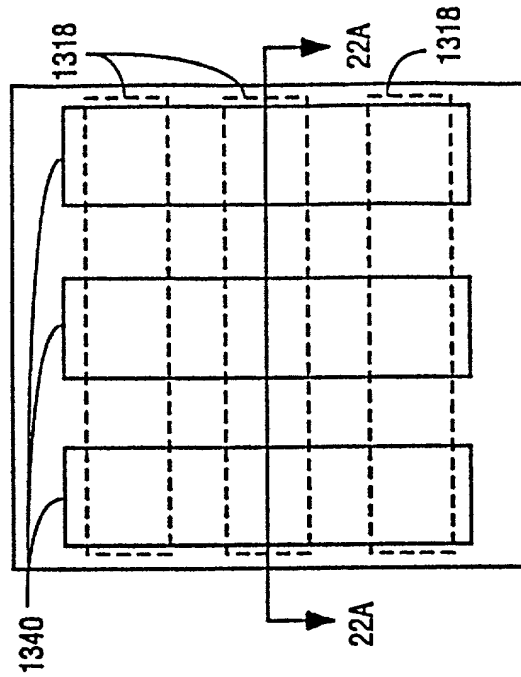


FIG. 22B

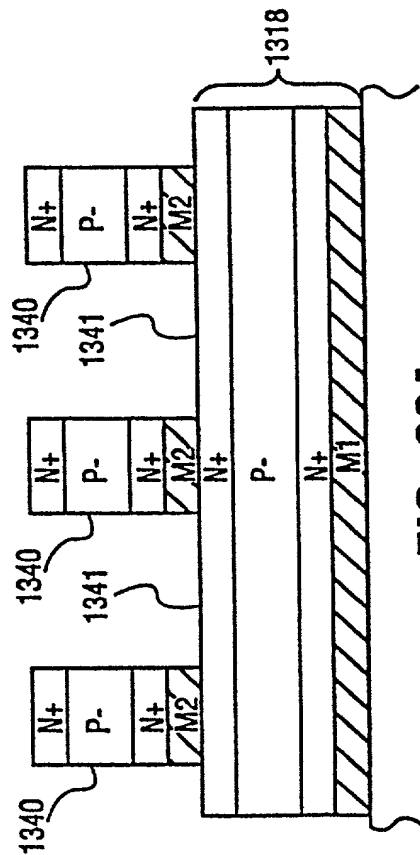


FIG. 22A



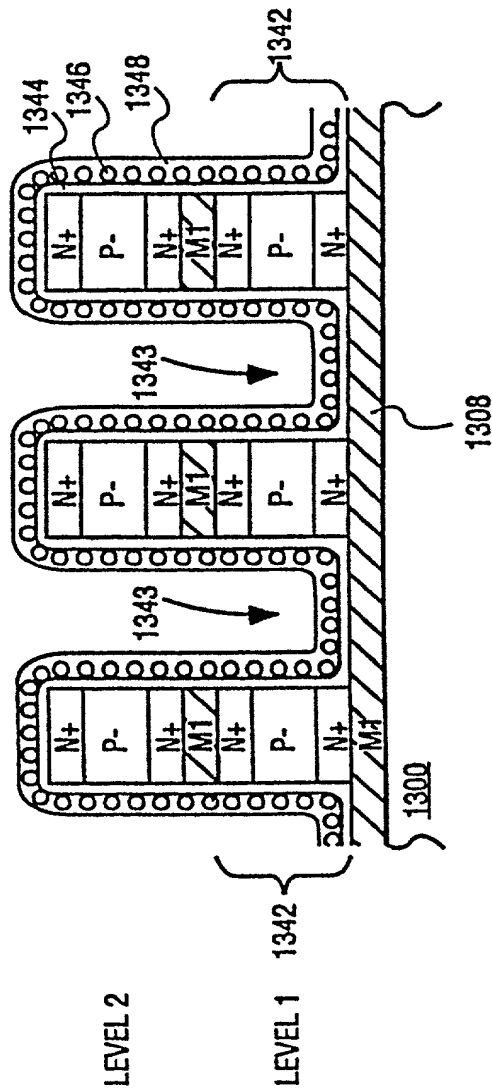


FIG. 24

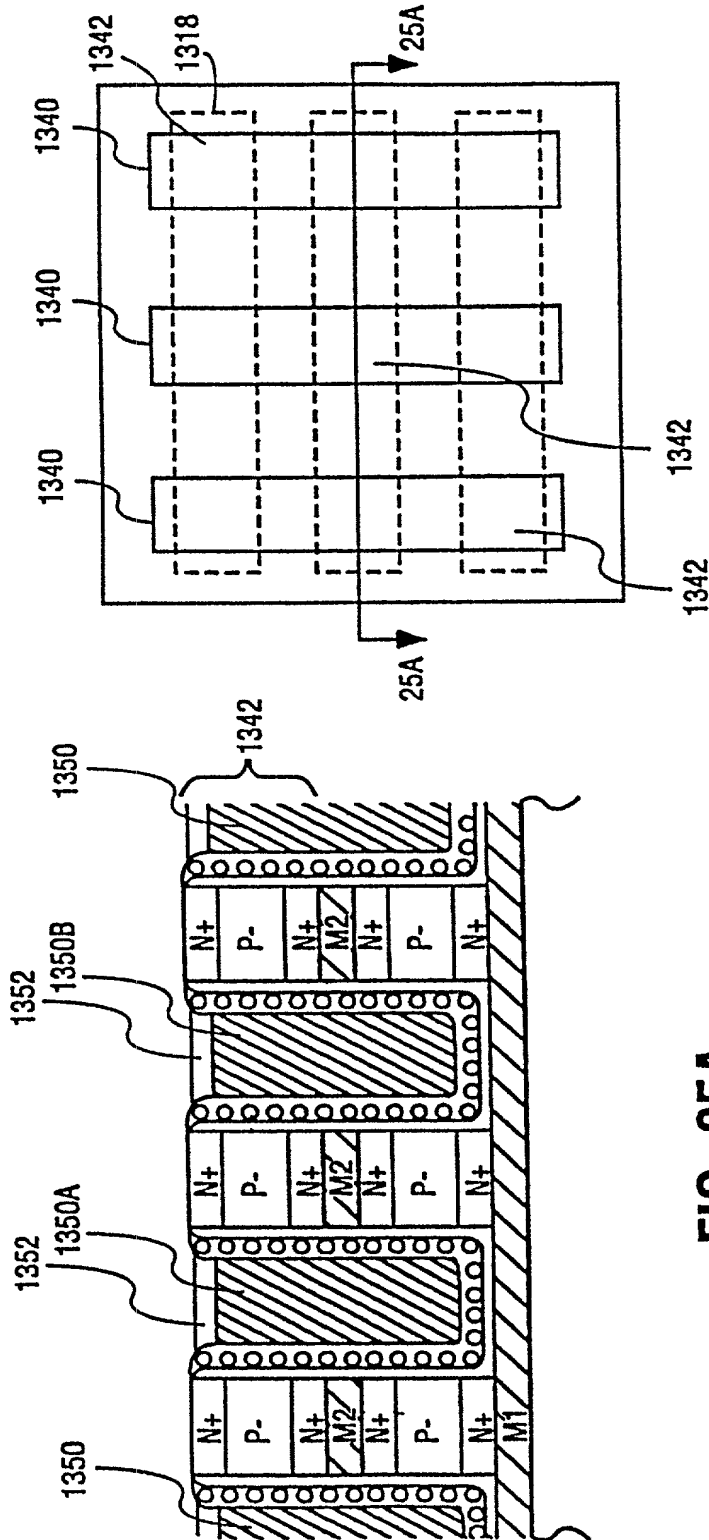


FIG. 25A

FIG. 25B

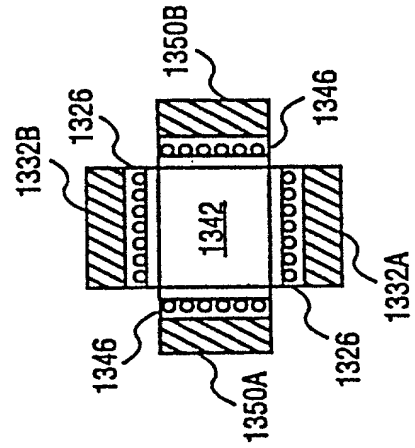
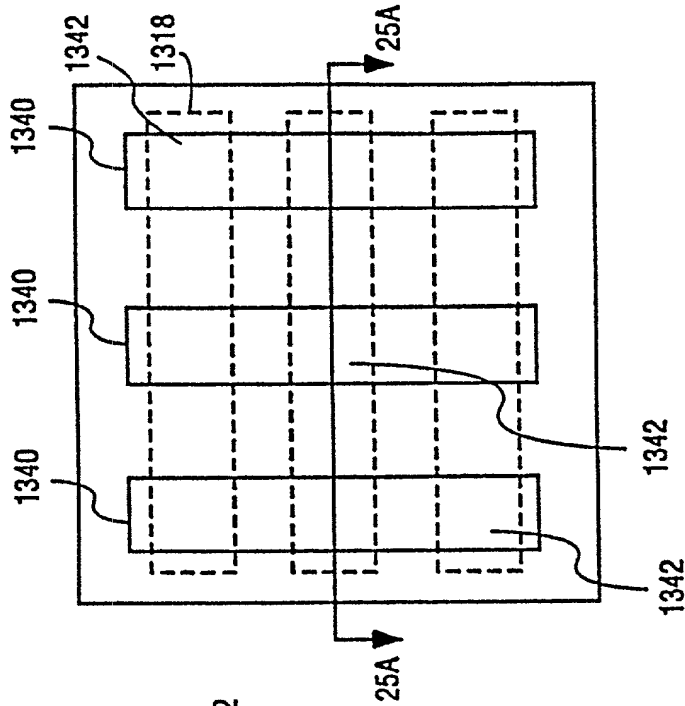


FIG. 26

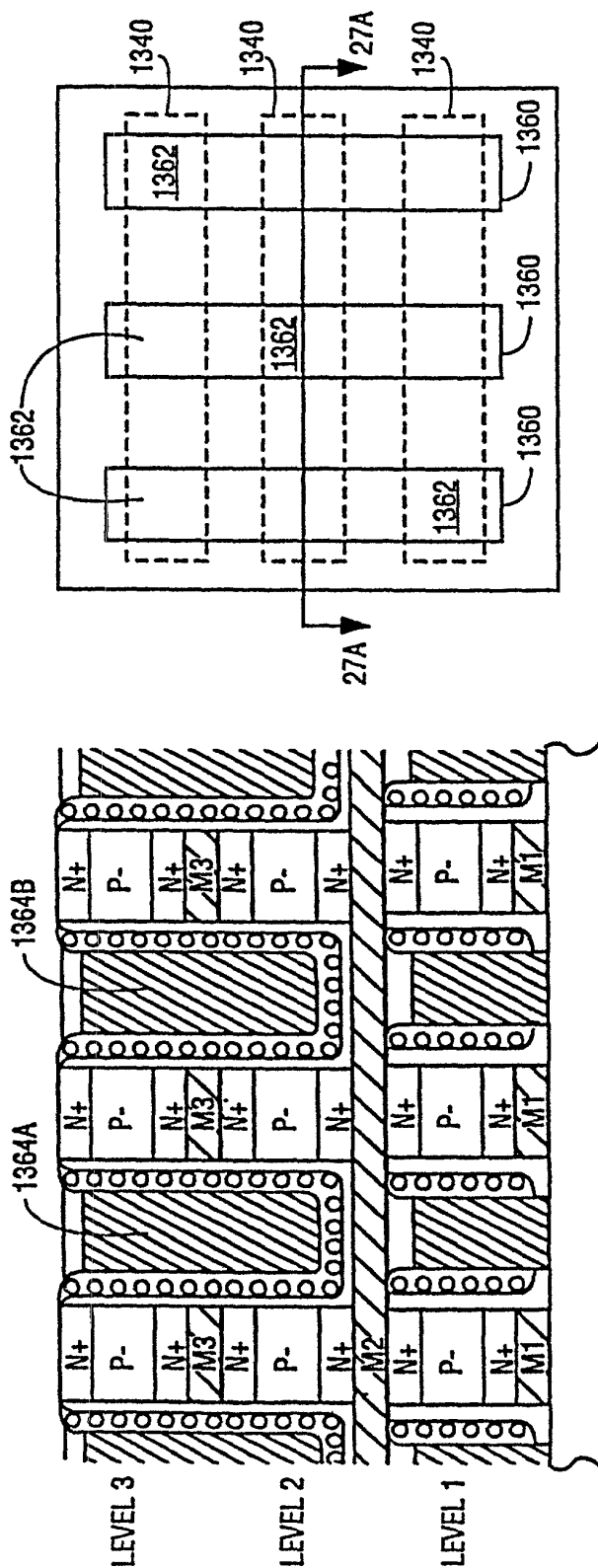


FIG. 27B

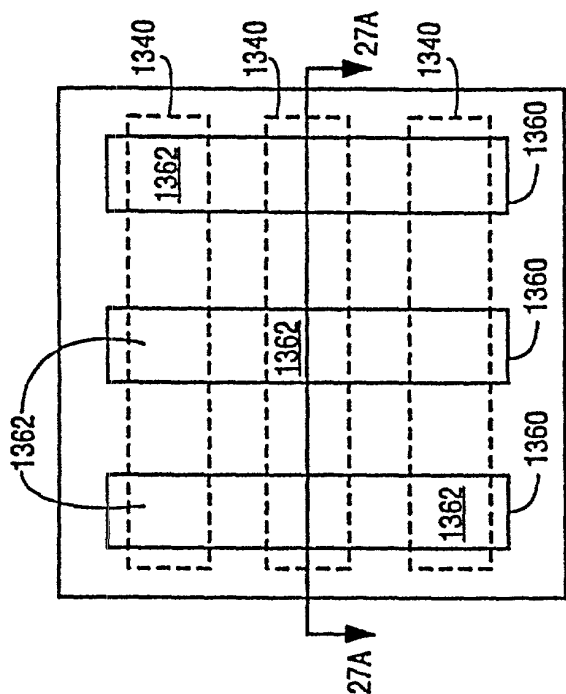


FIG. 27A

FIG. 28

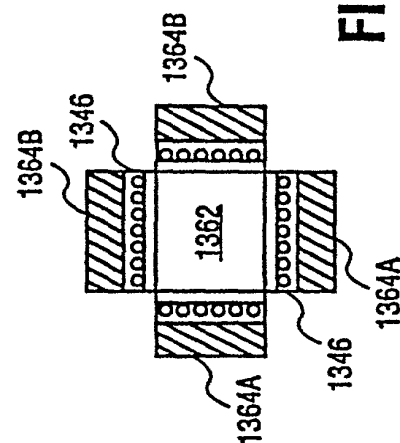


FIG. 29A

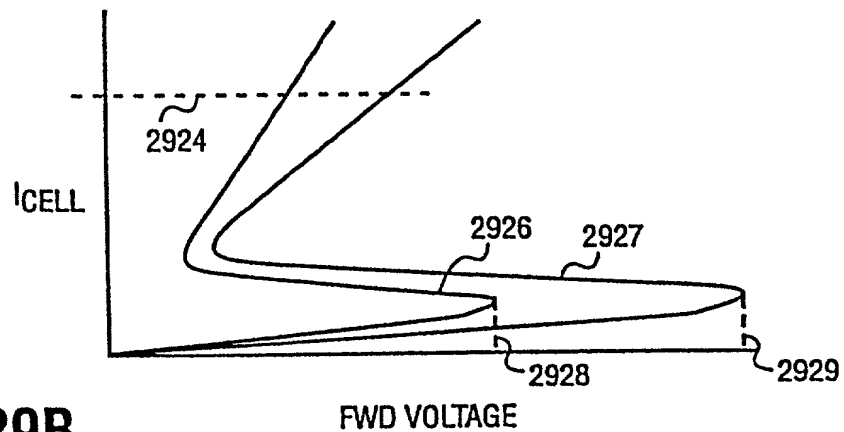
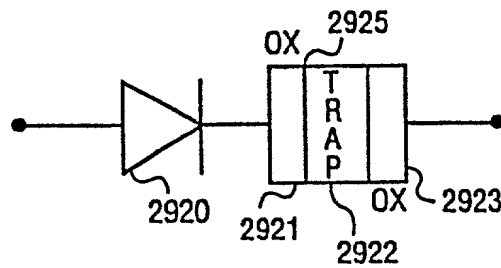


FIG. 29B

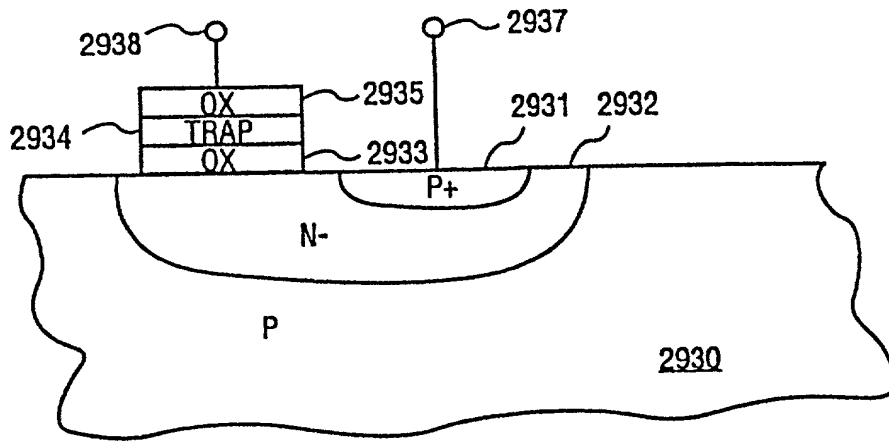


FIG. 30

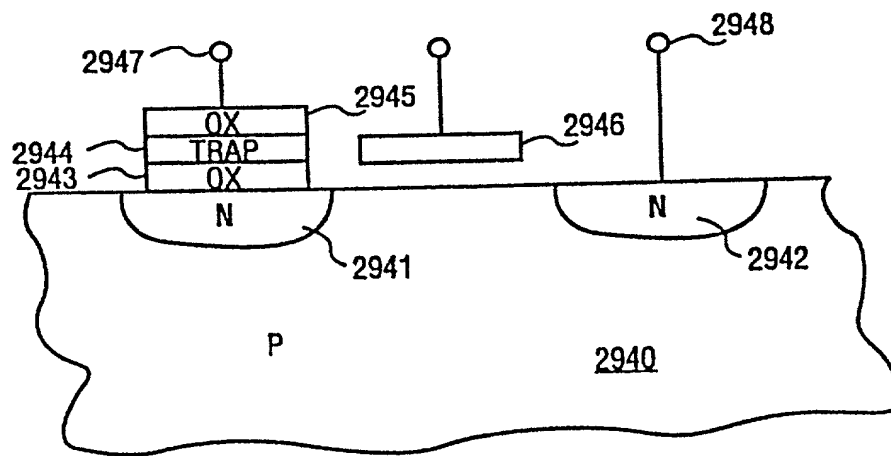
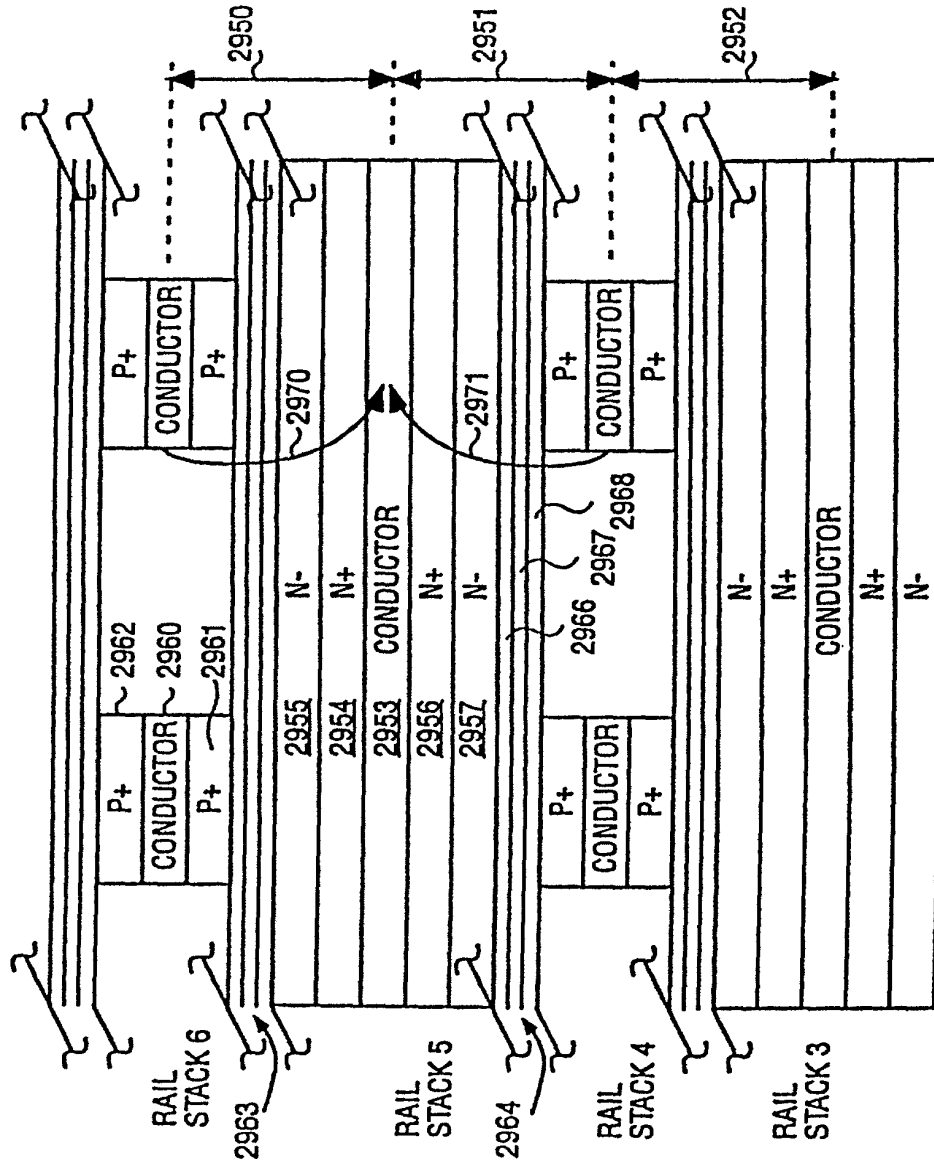


FIG. 31

FIG. 32



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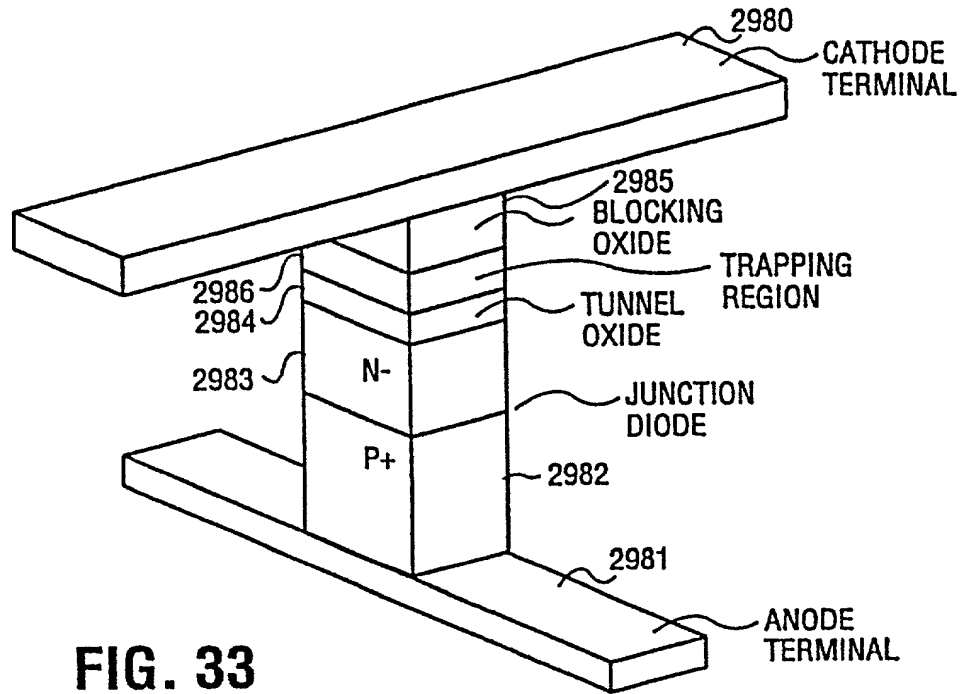


FIG. 33

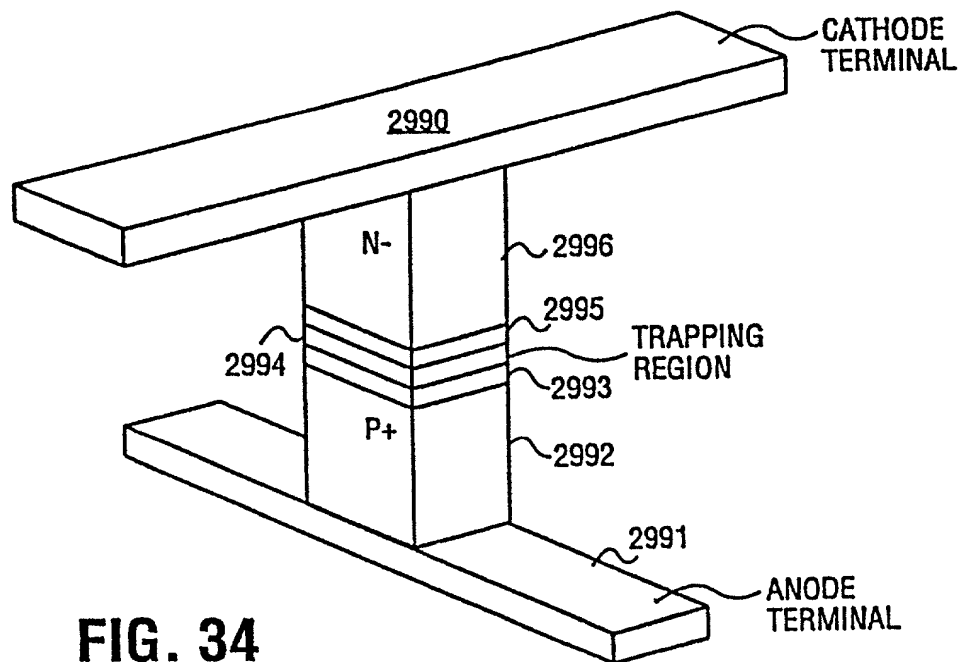


FIG. 34

FIG. 35

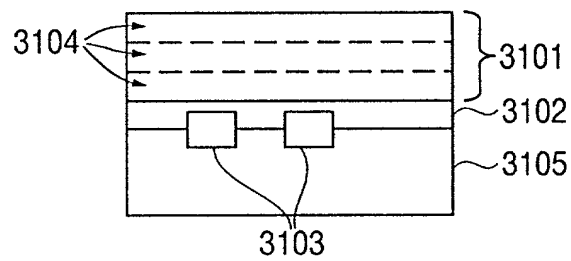


FIG. 36

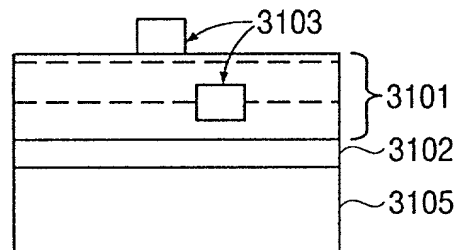


FIG. 37

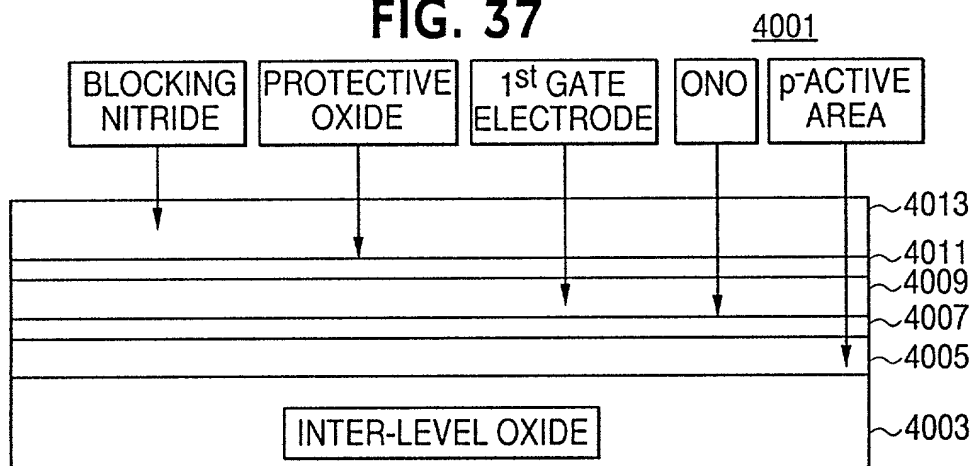
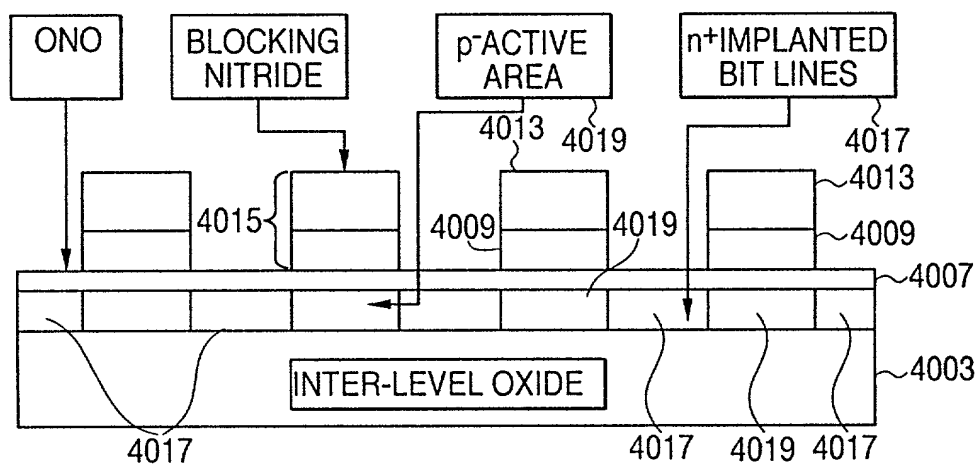


FIG. 38



This cross-sectional view illustrates a semiconductor device structure. A substrate 4003 is covered by a layer of inter-level oxide 4017. On top of the oxide, there are several conductive layers and spacers. A 1st GATE ELECTRODE 4007 is shown, along with an OXIDE SPACER 4021. TiSi2 IN BIT LINES 4023 are also present. The structure includes various conductive layers 4007, 4009, 4021, 4023, and 4025, which are interconnected by a network of lines. The inter-level oxide 4017 is shown as a continuous layer beneath the conductive structures.

[illegible]

FIG. 41

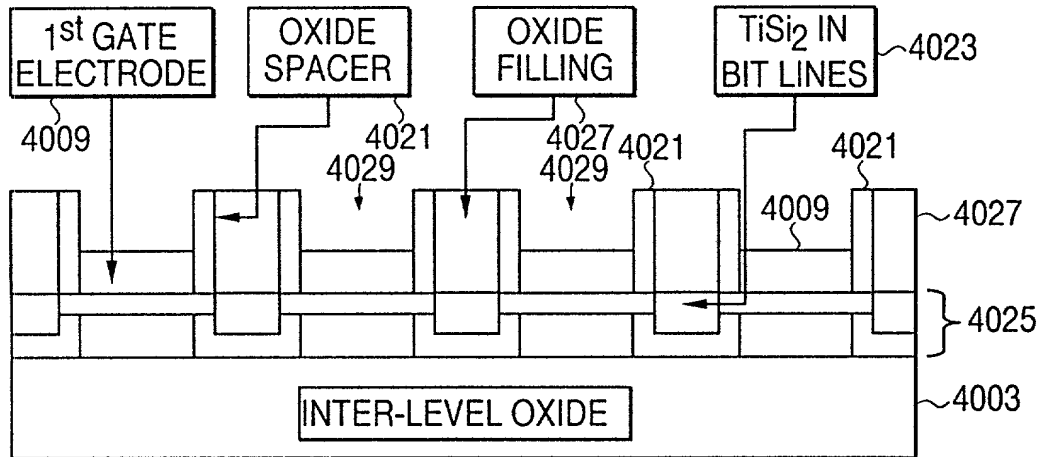


FIG. 42

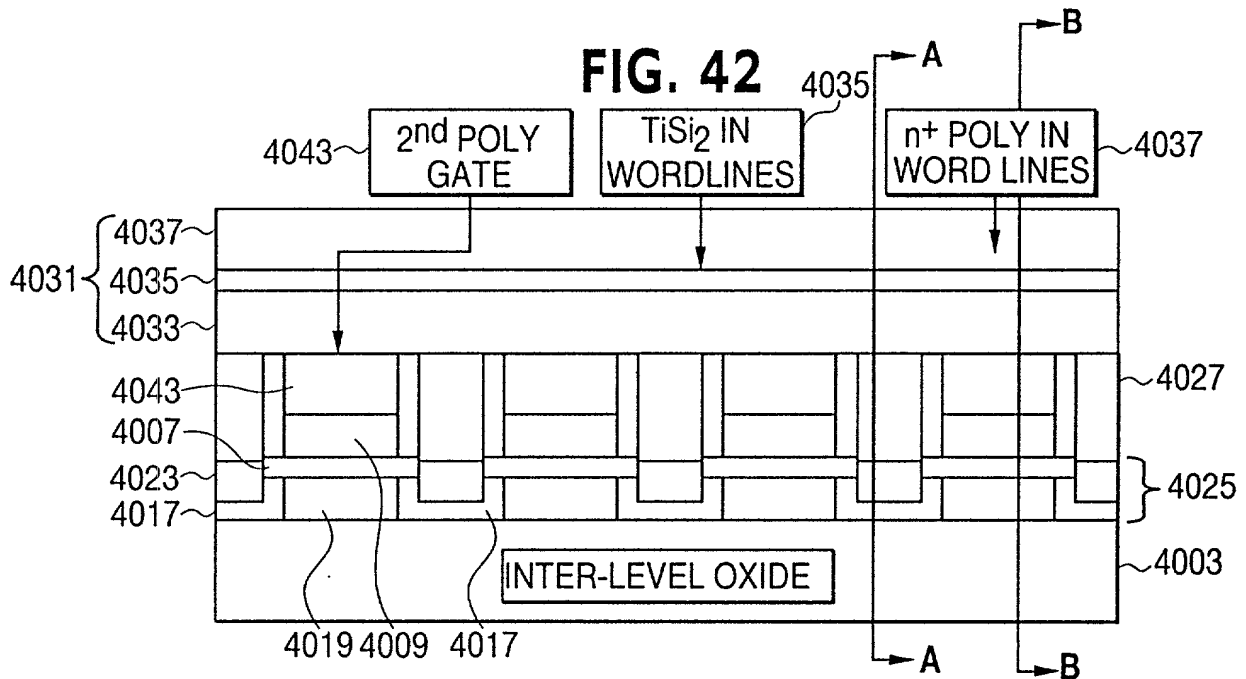


FIG. 43

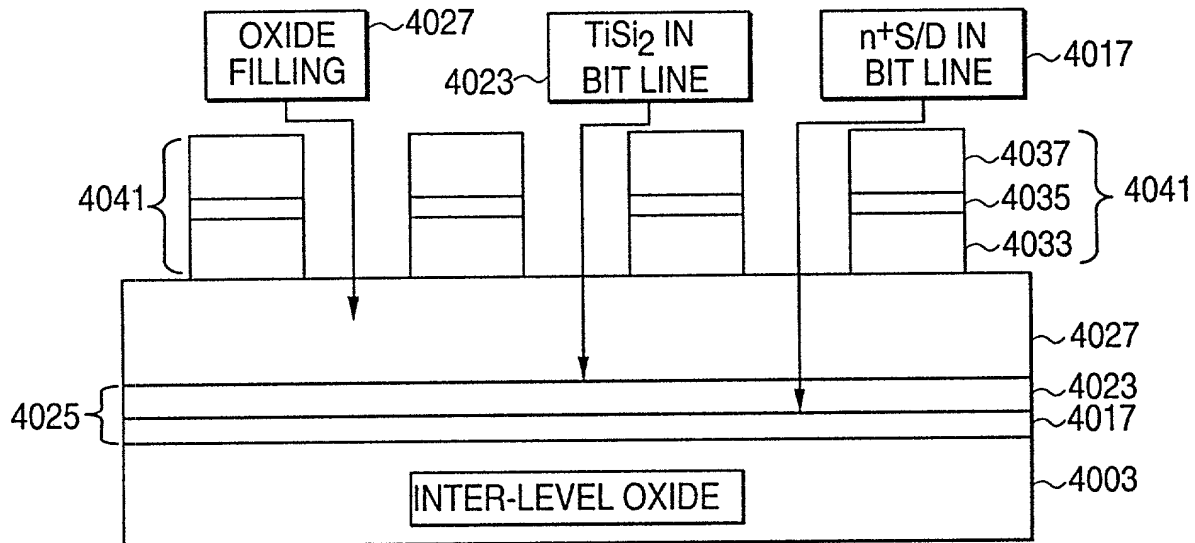


FIG. 44

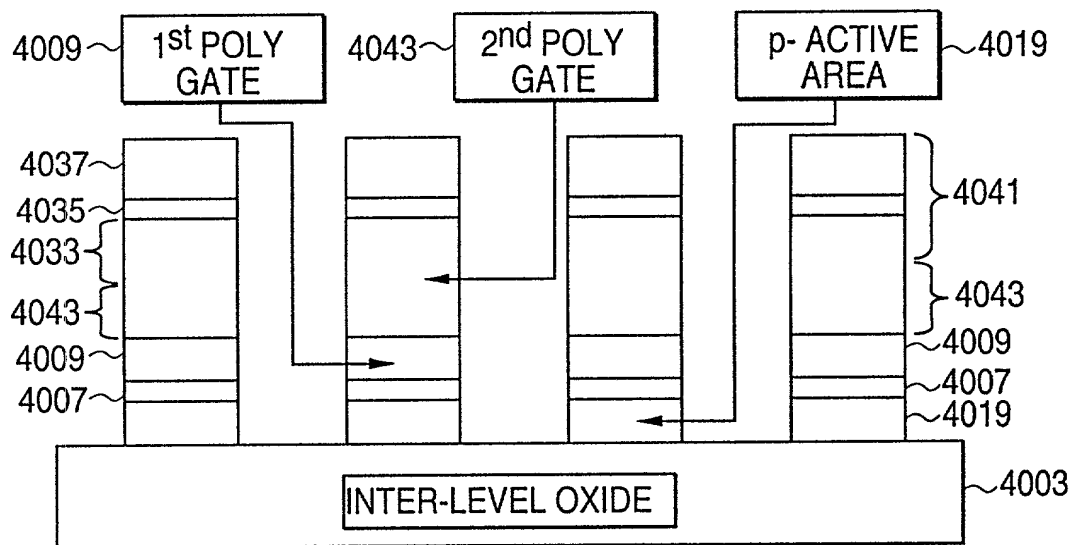


FIG. 45

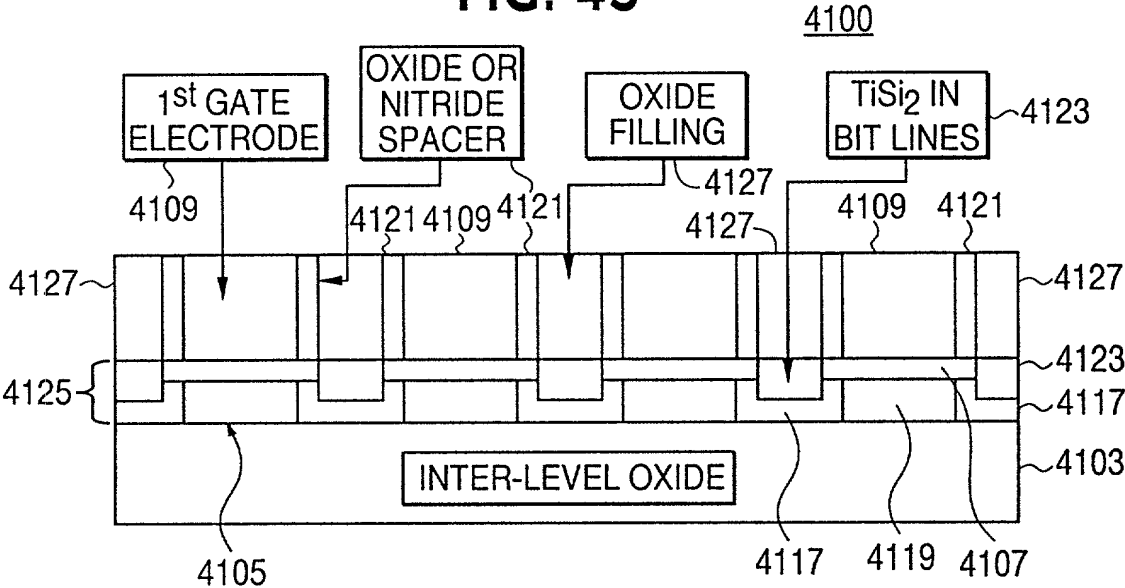


FIG. 46

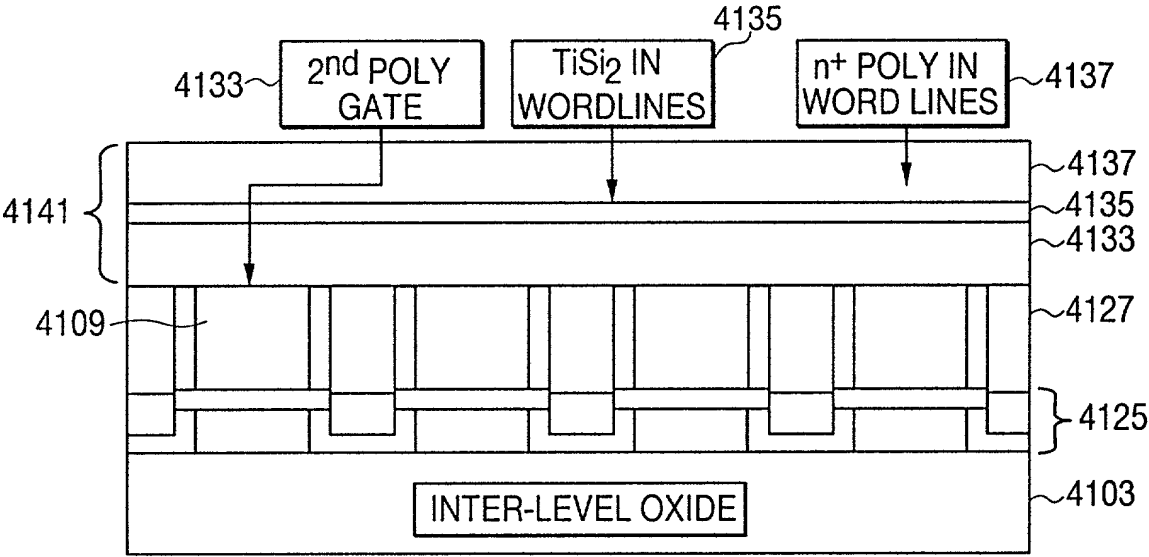


FIG. 47

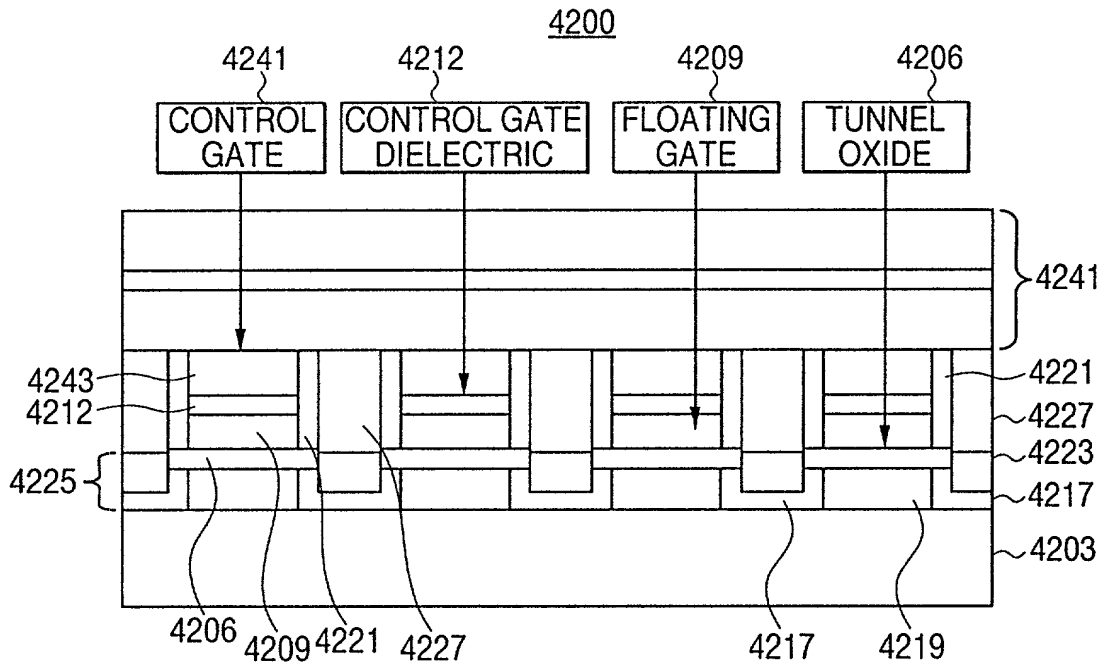


FIG. 48A

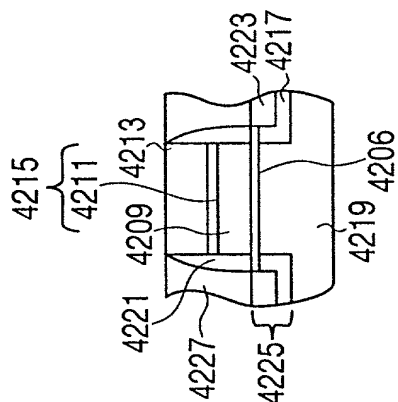


FIG. 48B

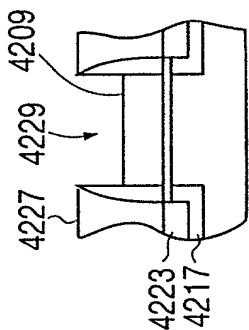


FIG. 48C

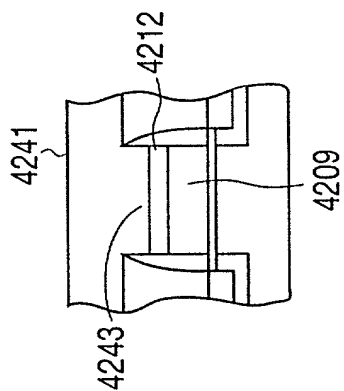


FIG. 49A

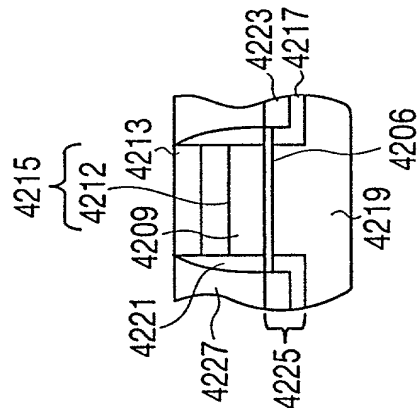


FIG. 49B

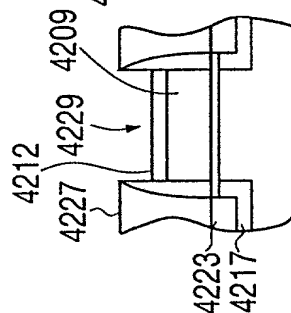


FIG. 49C

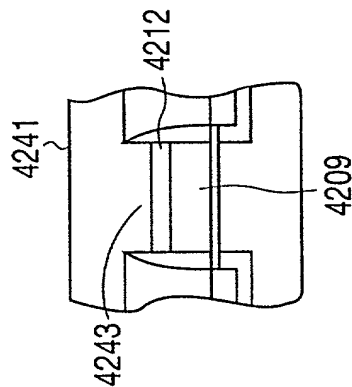


FIG. 50

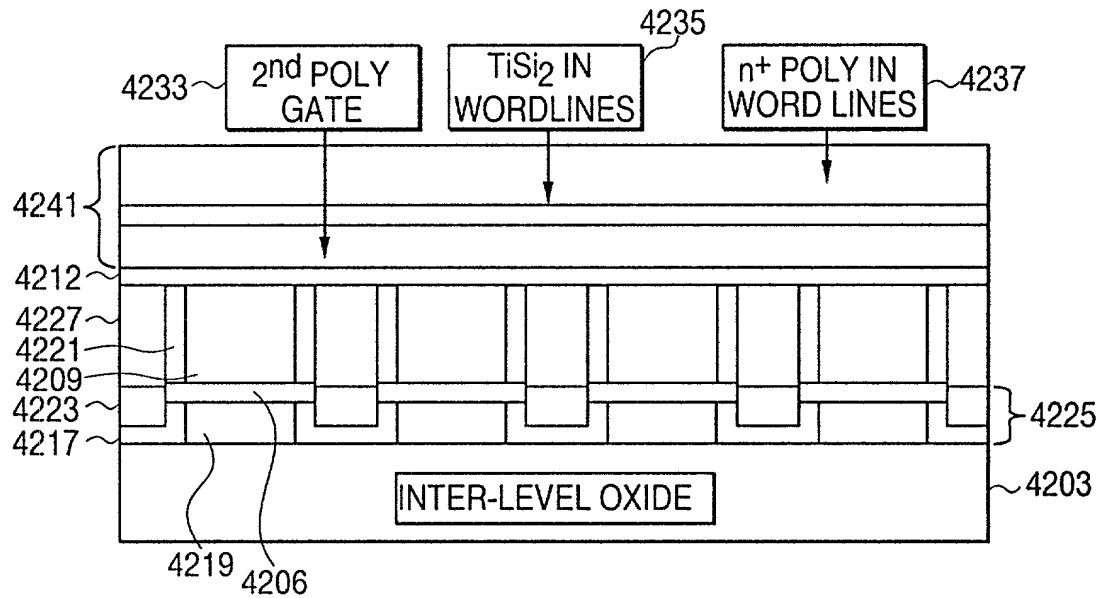


FIG. 51

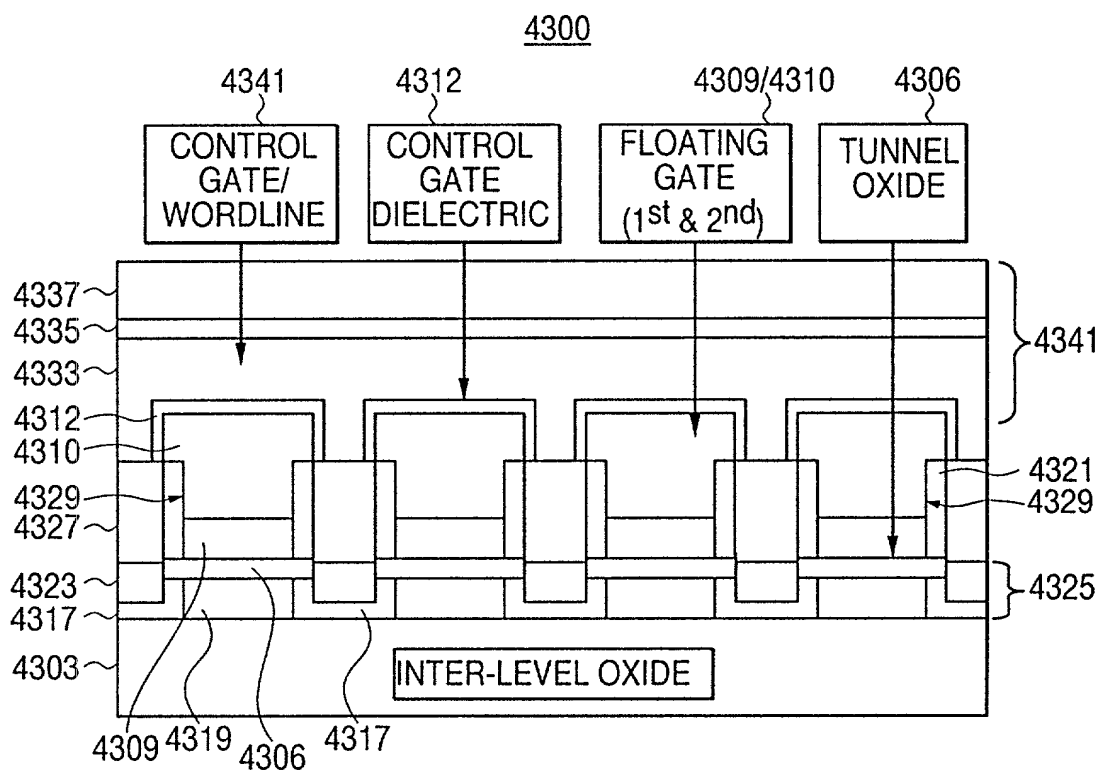


FIG. 52

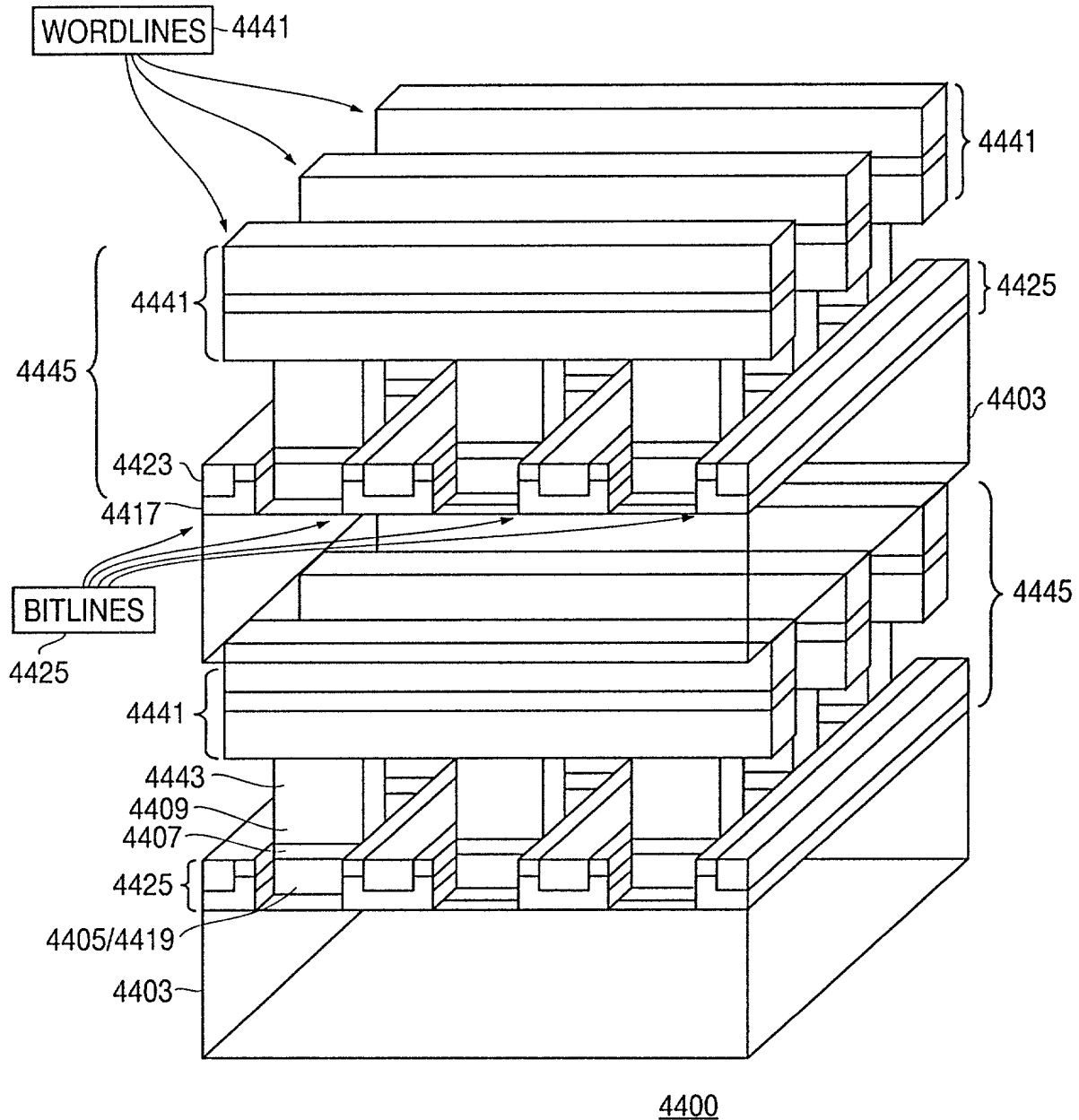


FIG. 53

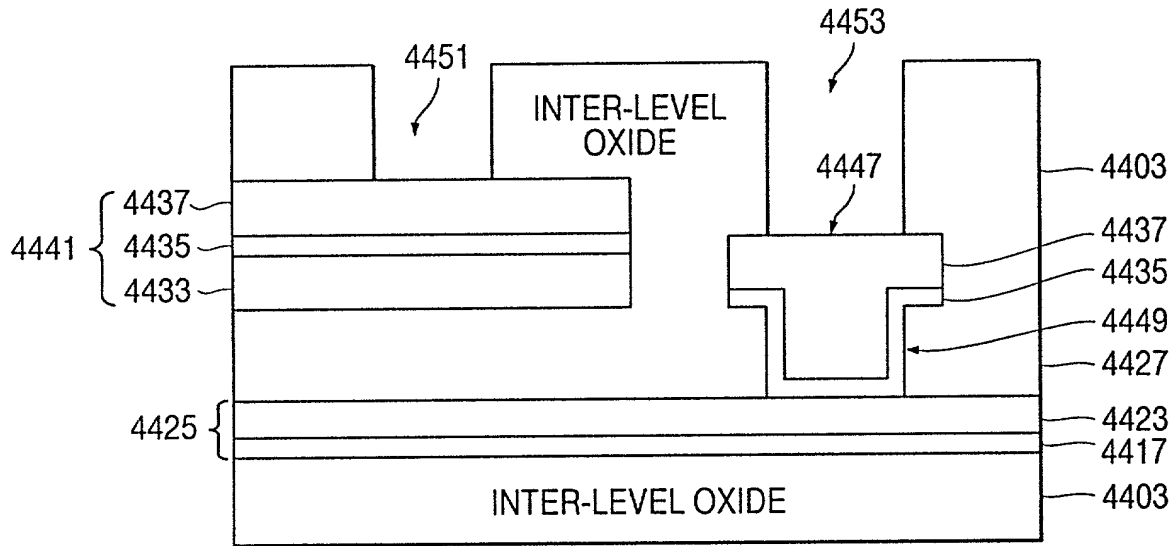


FIG. 54

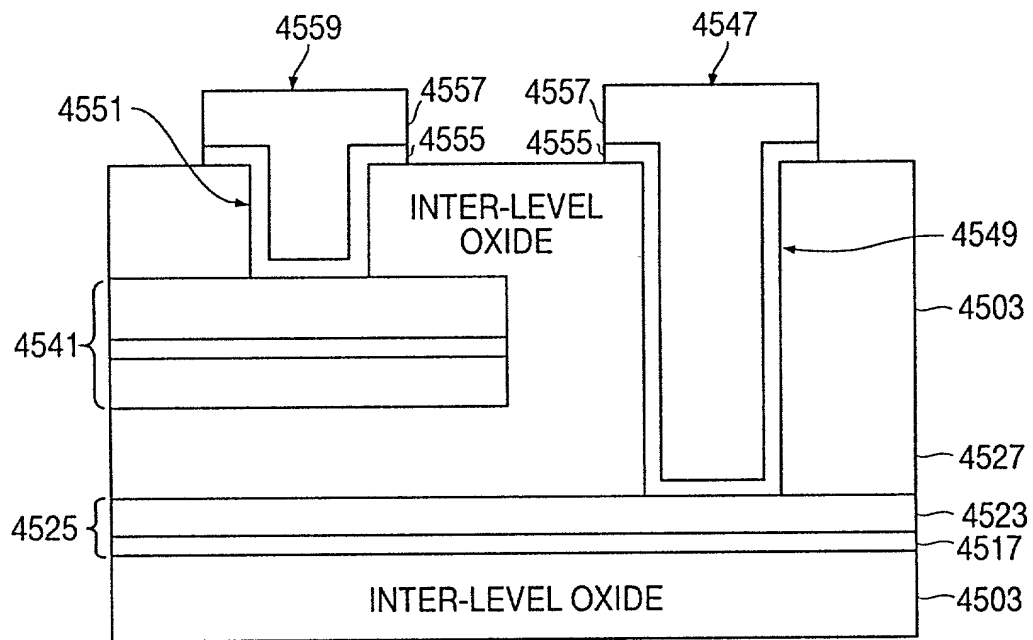


FIG. 55

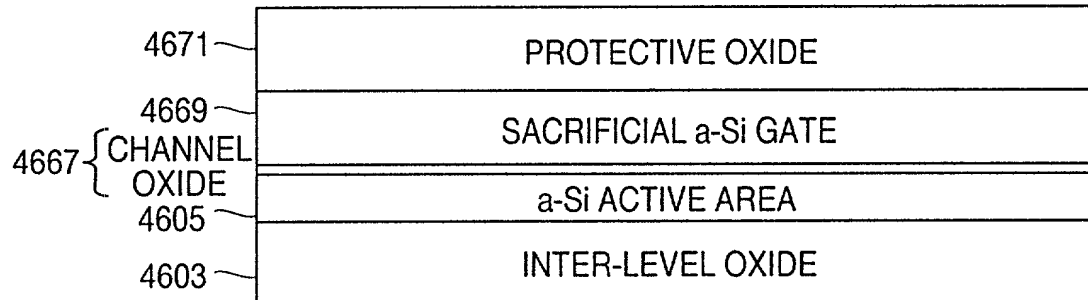


FIG. 56

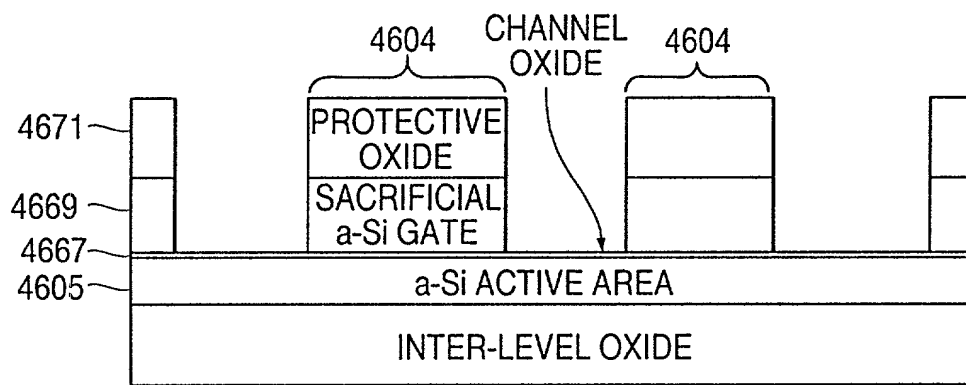
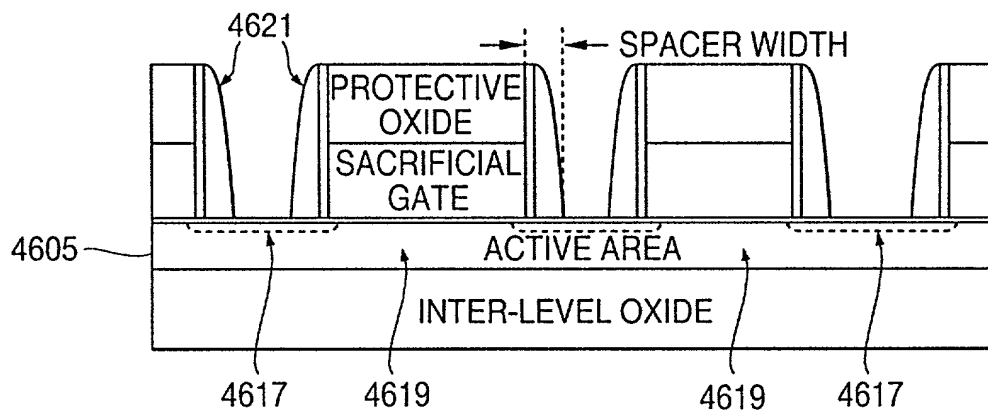


FIG. 57



A cross-sectional view of a semiconductor device. The structure consists of a substrate (4603) with an inter-level oxide layer (4605) on top. A poly-silicon active area (4617) is formed in the substrate. A sacrificial gate (4609) is formed on the active area, with salicide in bit lines (4623) on top. The sacrificial gate is surrounded by HDP oxide (4621). The active area is also surrounded by HDP oxide (4627). The active area is labeled 4619.

A cross-sectional view of a semiconductor device. The structure consists of a substrate with a thick layer of **Poly-Si ACTIVE AREA** at the bottom. Above this is a layer of **INTER-LEVEL OXIDE**. On top of the inter-level oxide, there are three raised regions. Each raised region has a central **HDP OXIDE** layer and is flanked by **4621** (HDP oxide) and **4627** (HDP oxide) layers. The top surface of the raised regions is labeled **4629**. The bit lines are labeled **4623 SALICIDE IN BIT LINES**.

FIG. 60

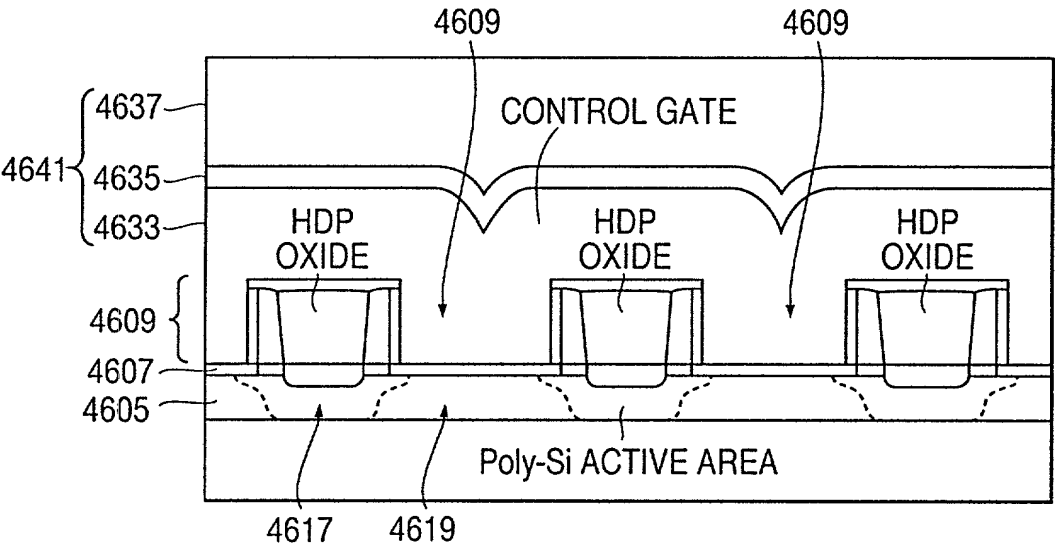


FIG. 61

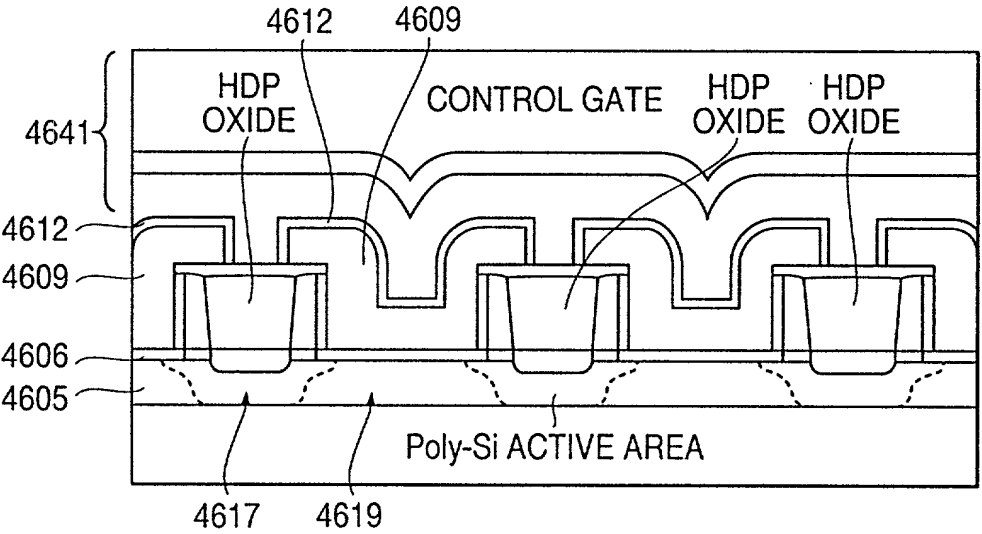


FIG. 62

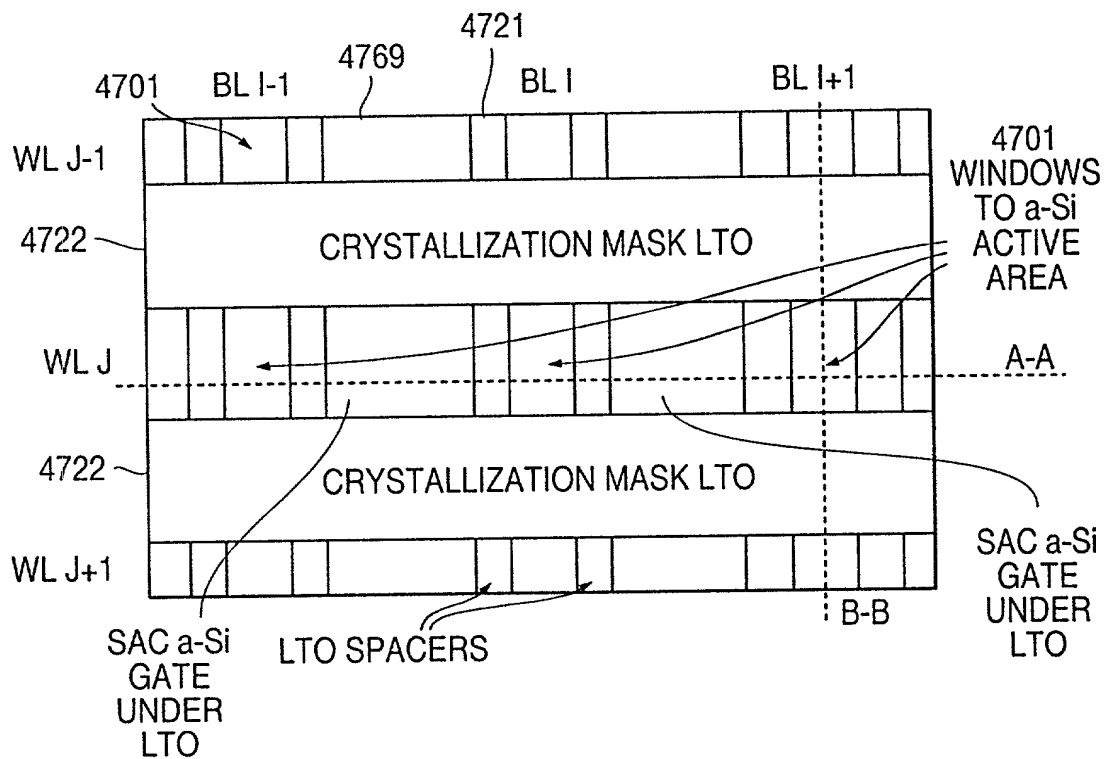


FIG. 63

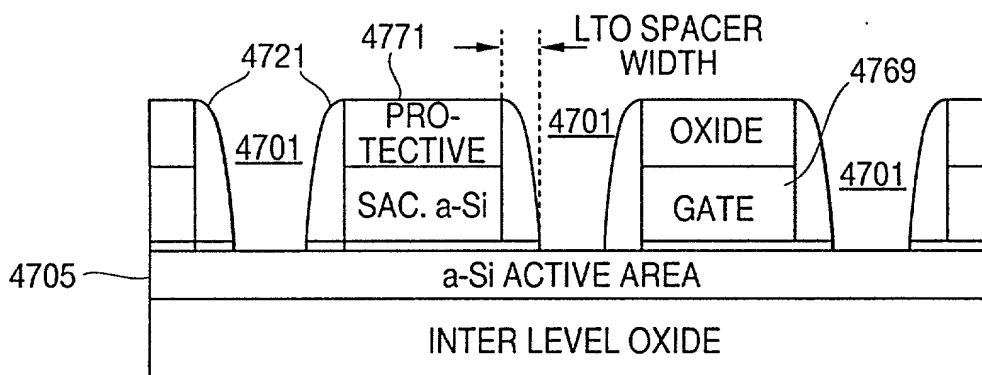


FIG. 64

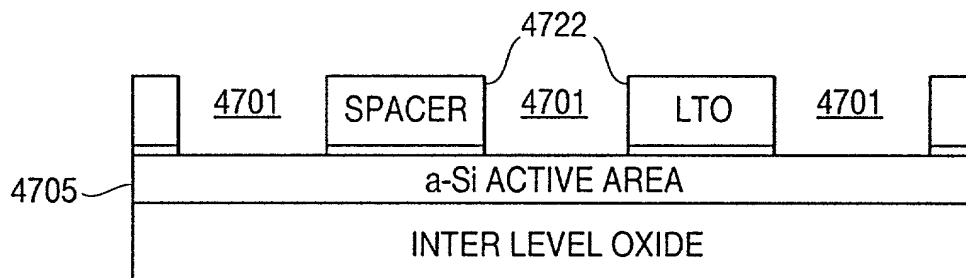


FIG. 65

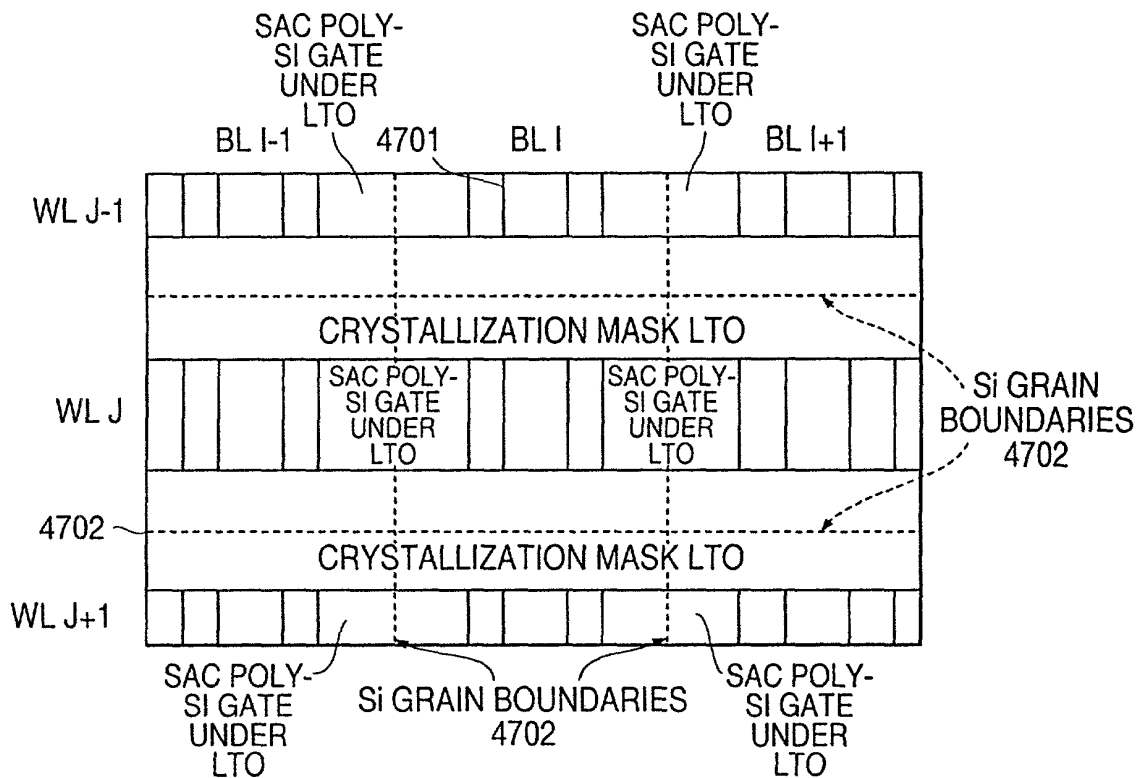
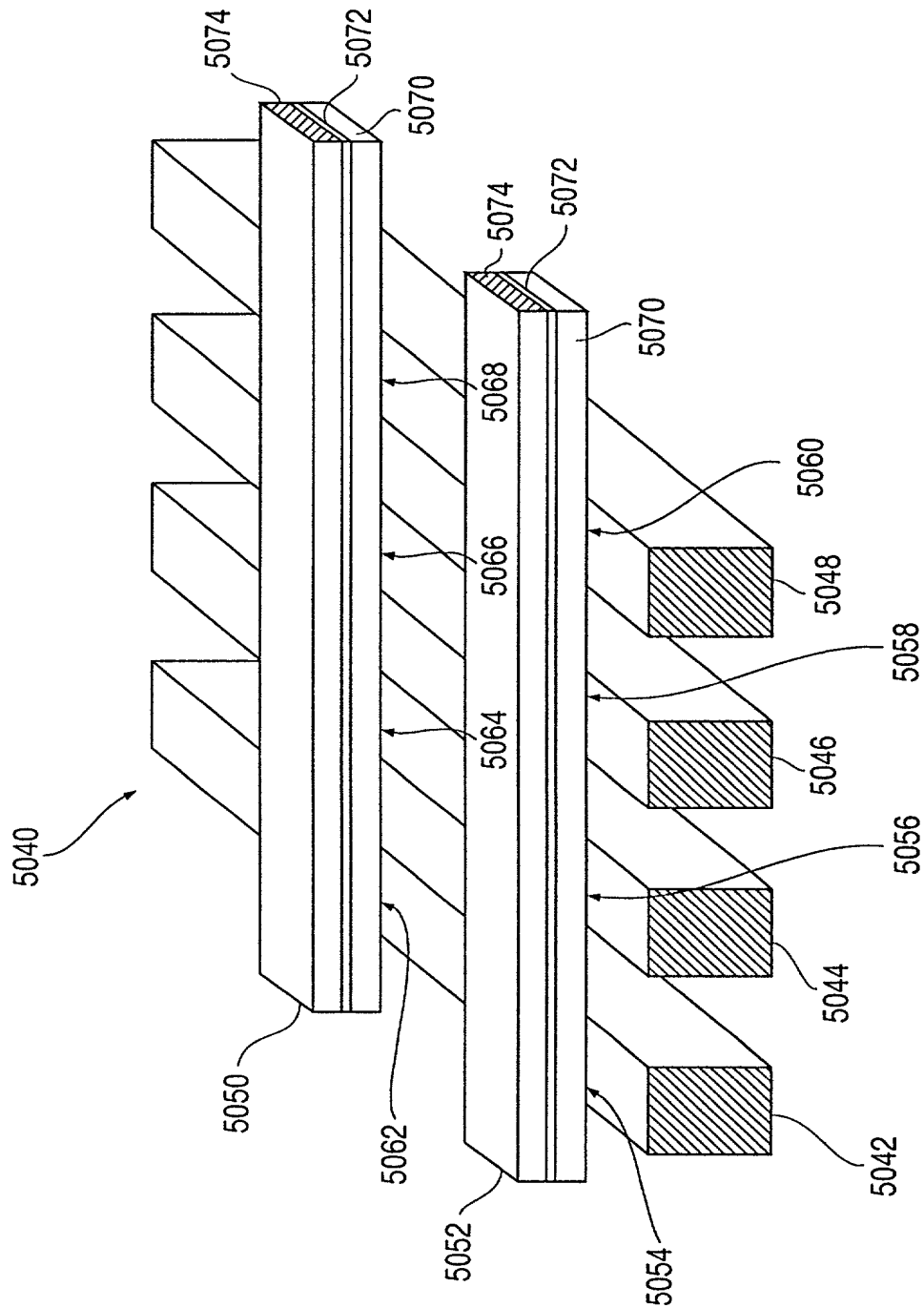


FIG. 66



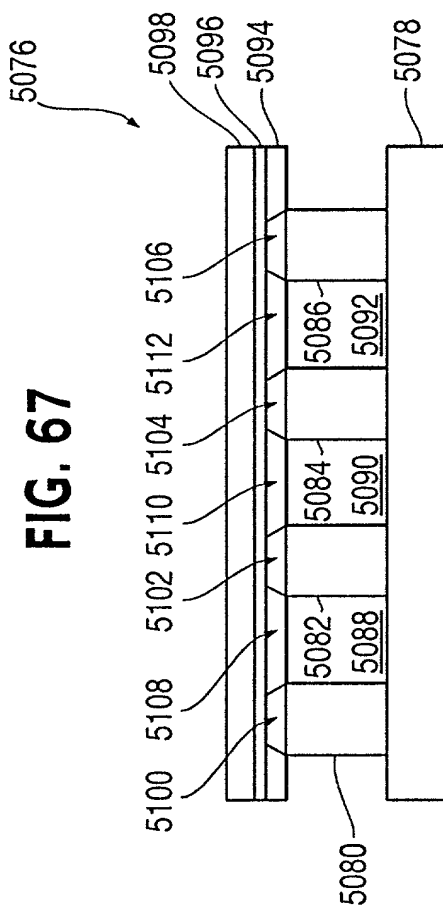


FIG. 68

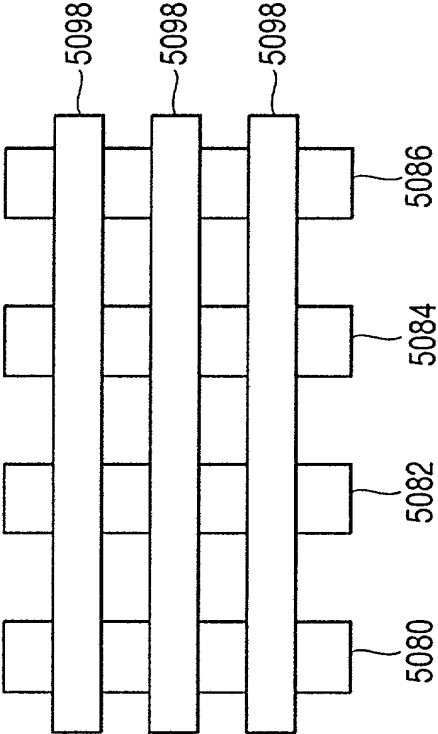


FIG. 69

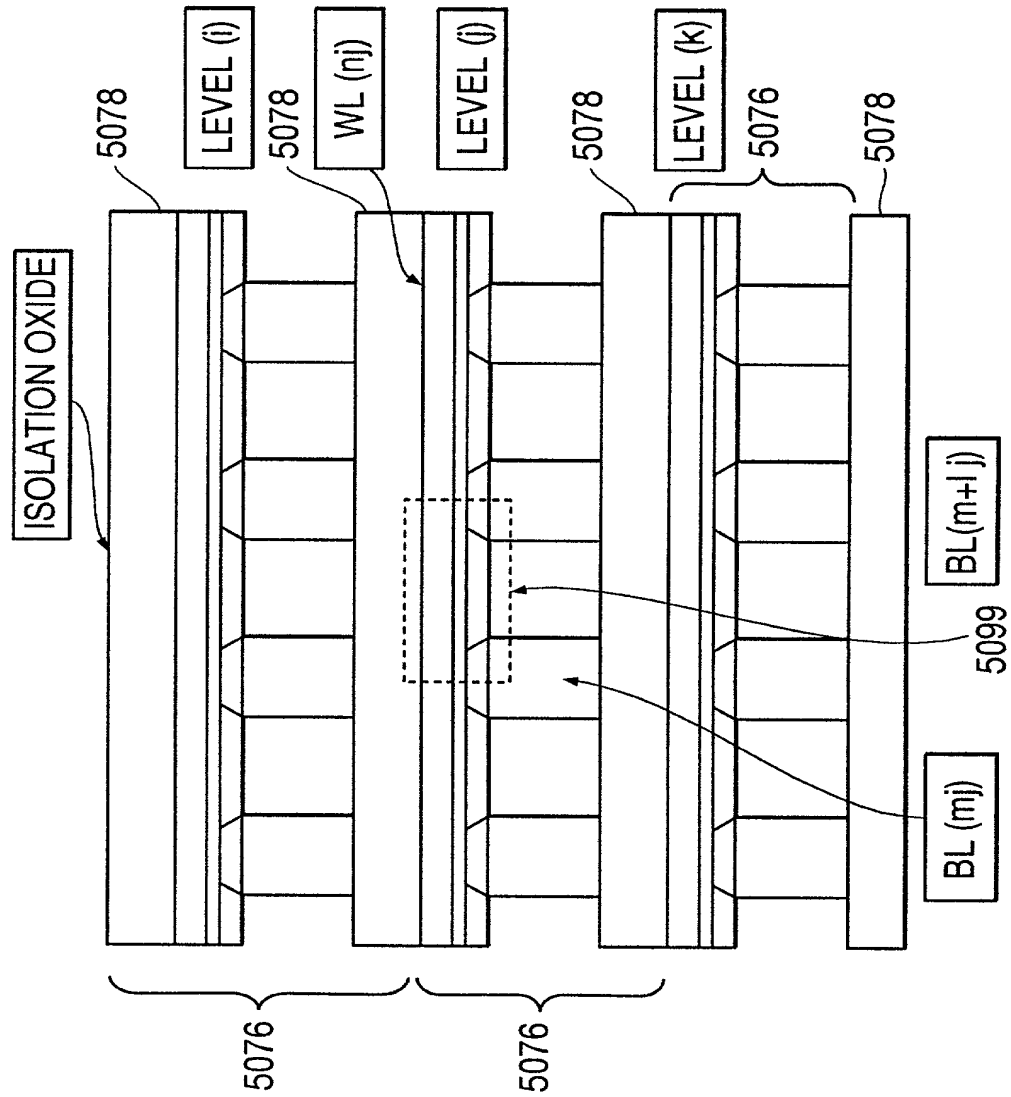


FIG. 70

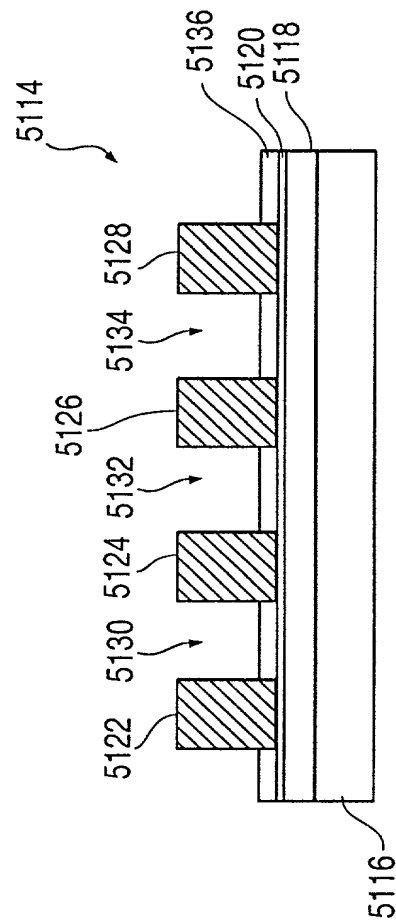


FIG. 71

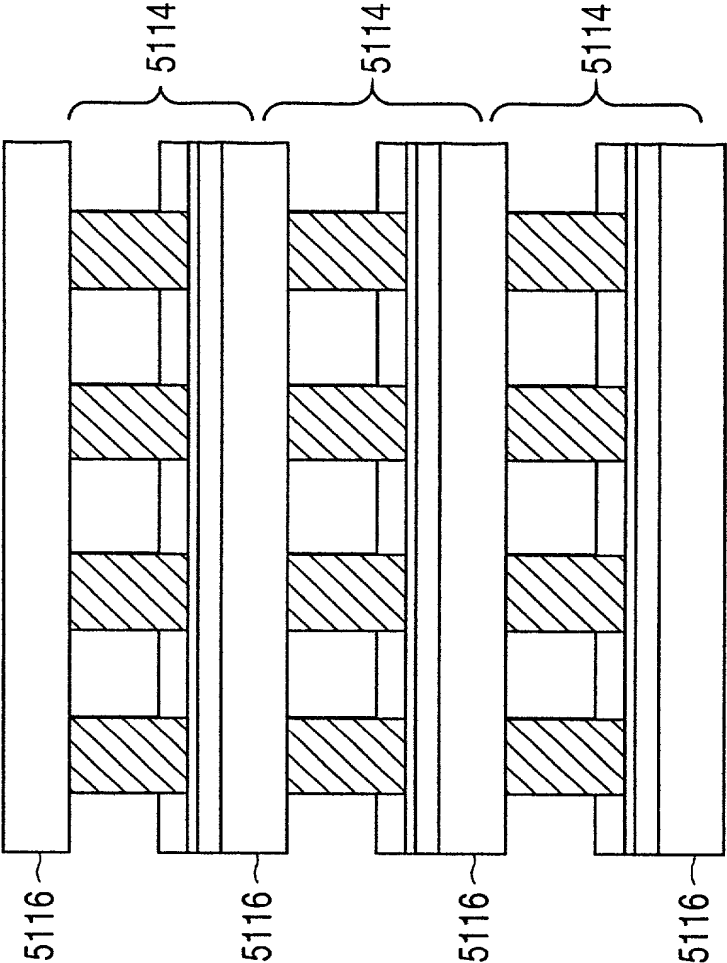


FIG. 72

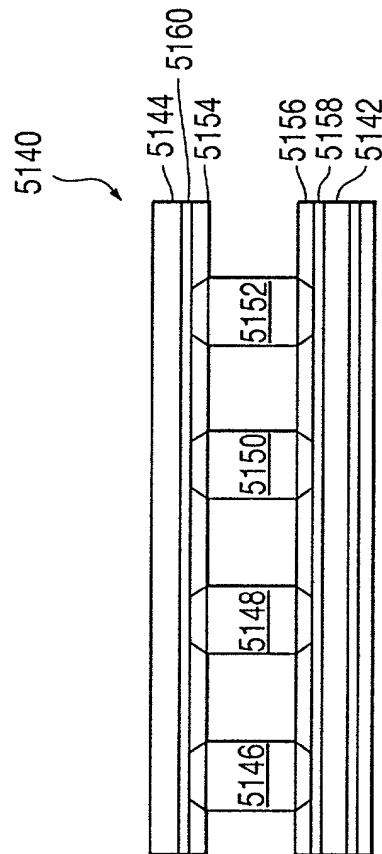


FIG. 73

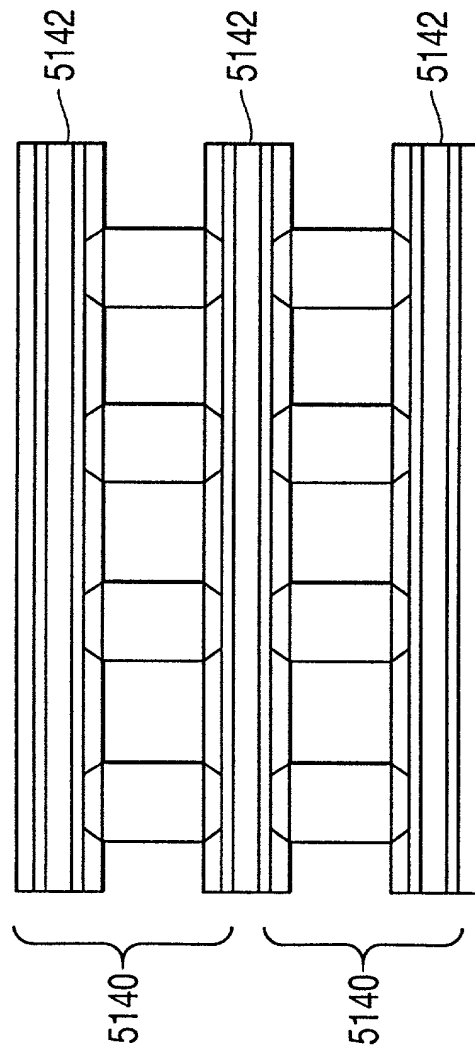


FIG. 74

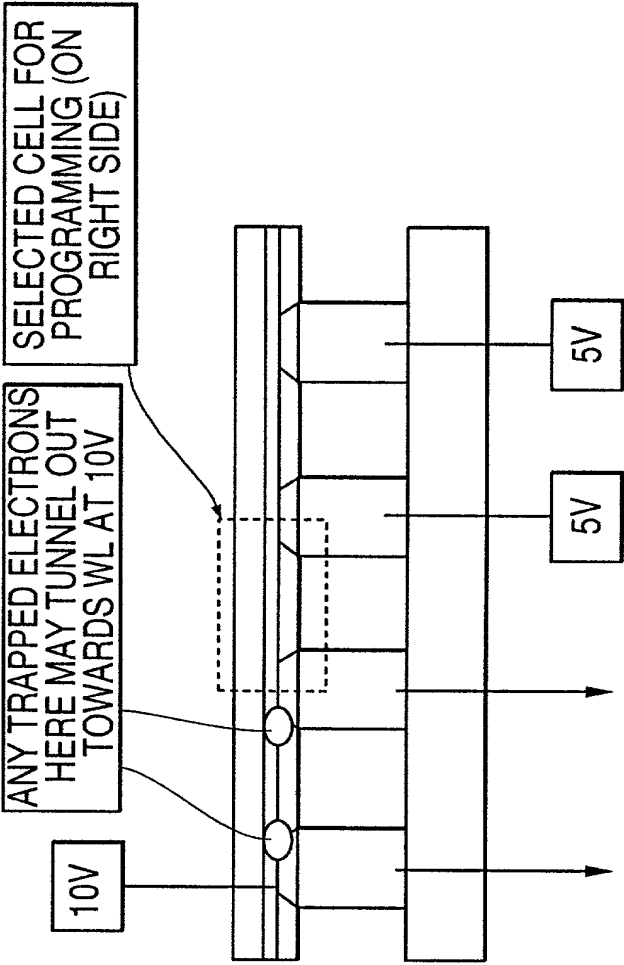


FIG. 75

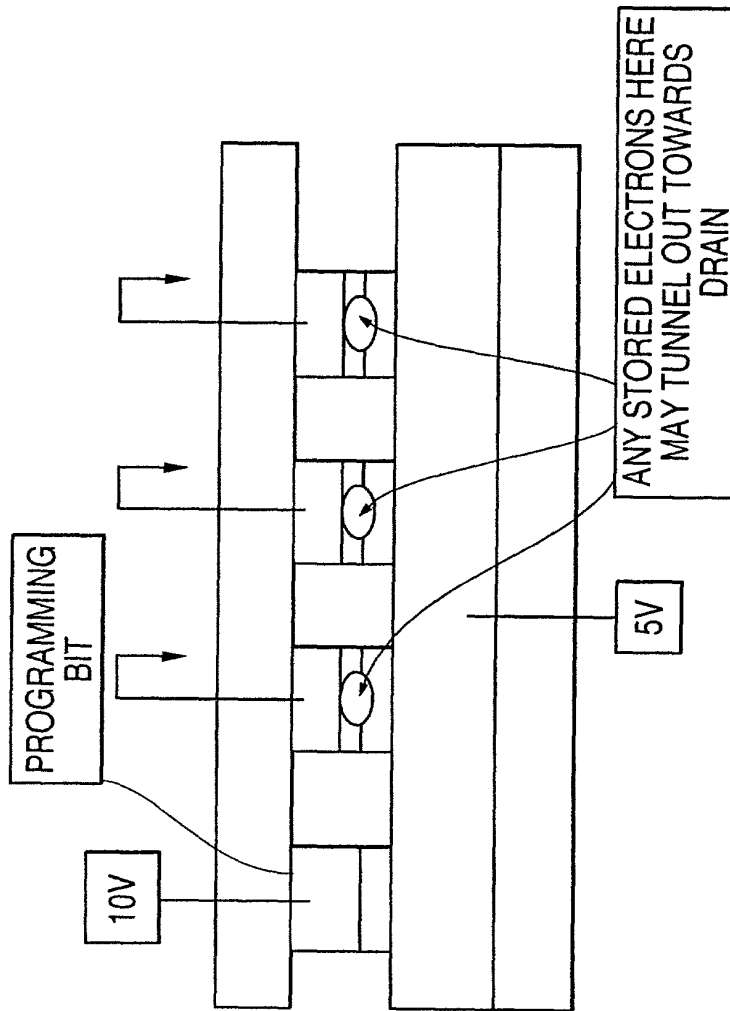


FIG. 76

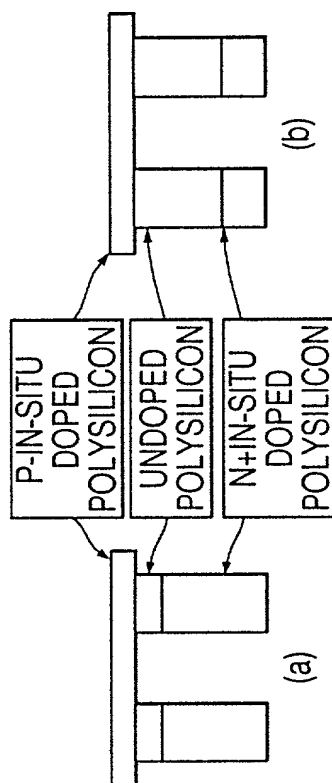


FIG. 77

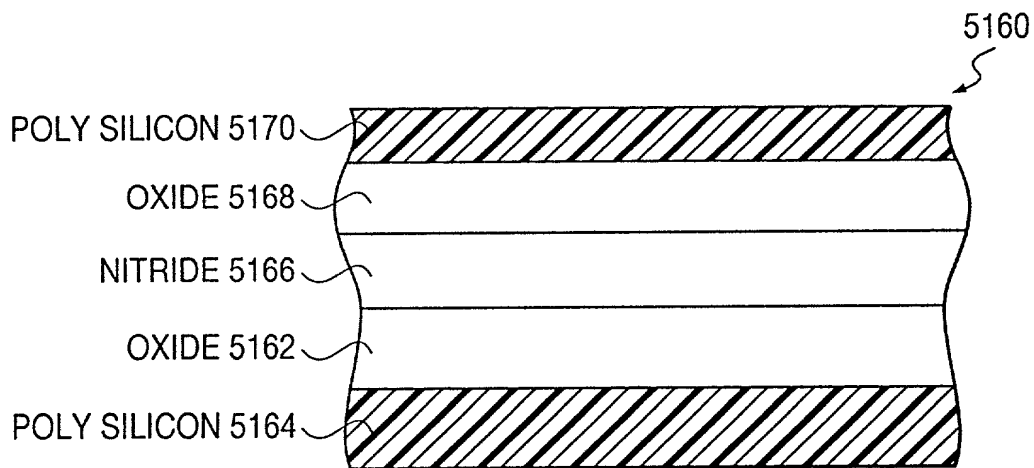


FIG. 80

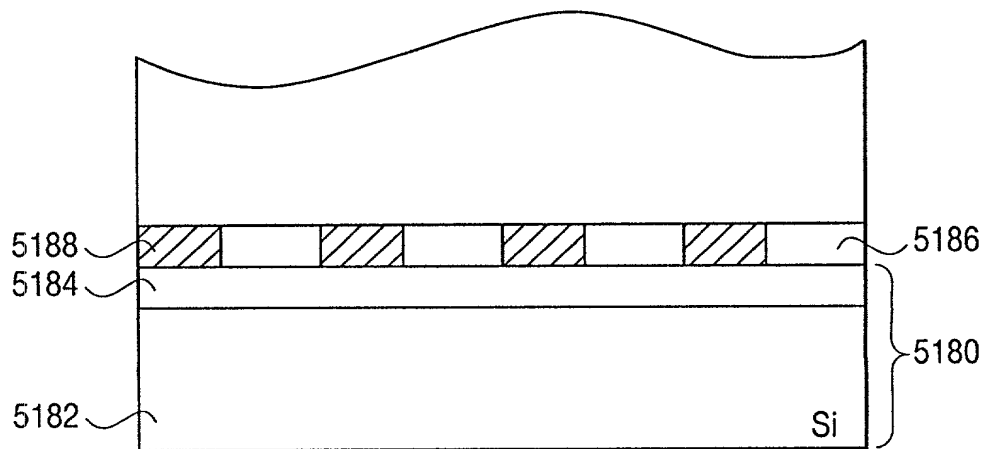


FIG. 78

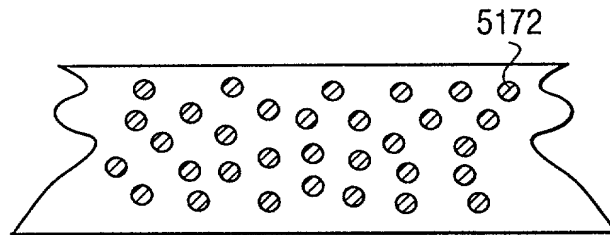


FIG. 79

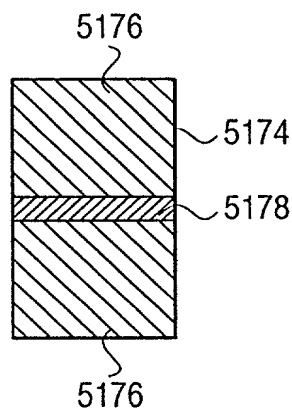


FIG. 81A

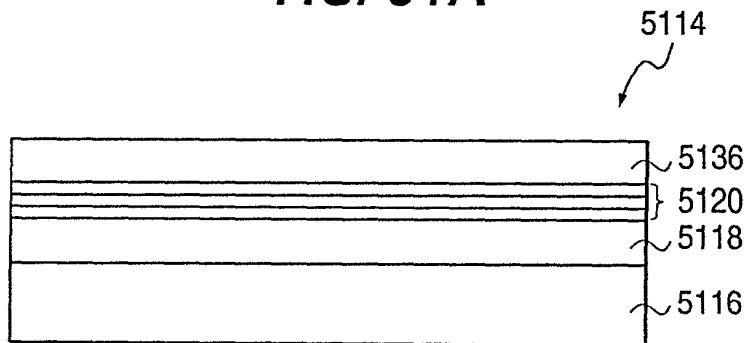


FIG. 81B

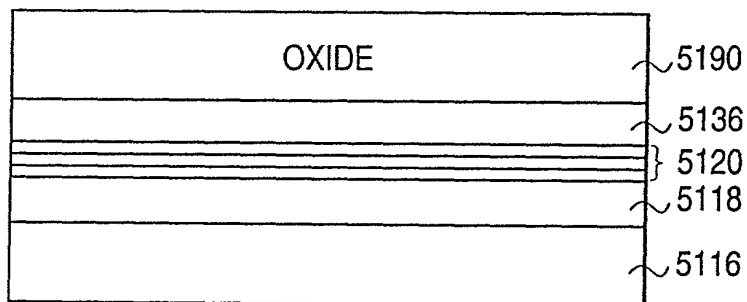


FIG. 81C

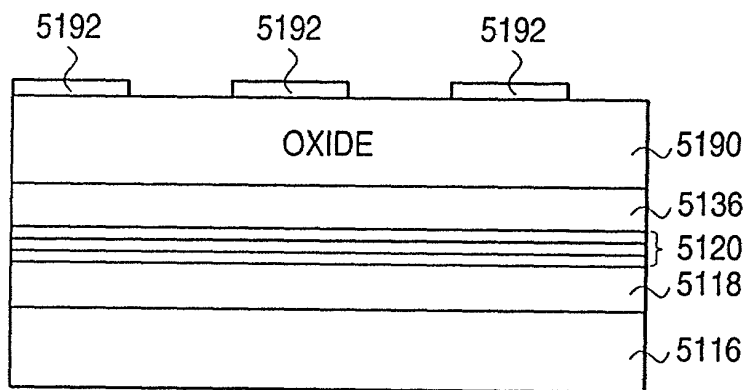


FIG. 81D

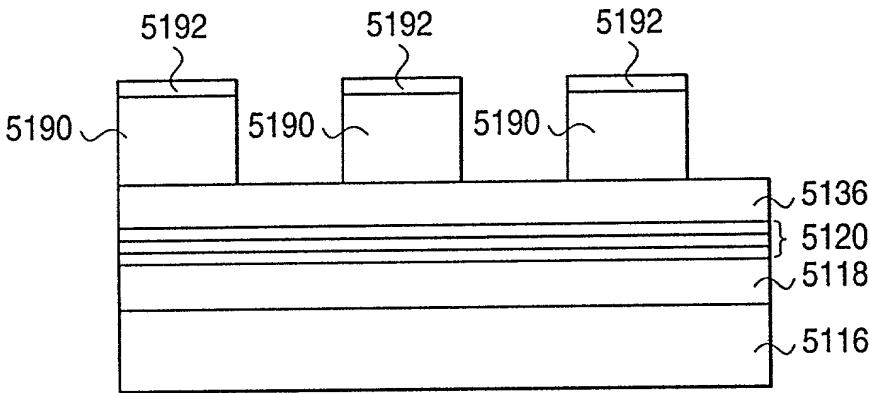


FIG. 81E

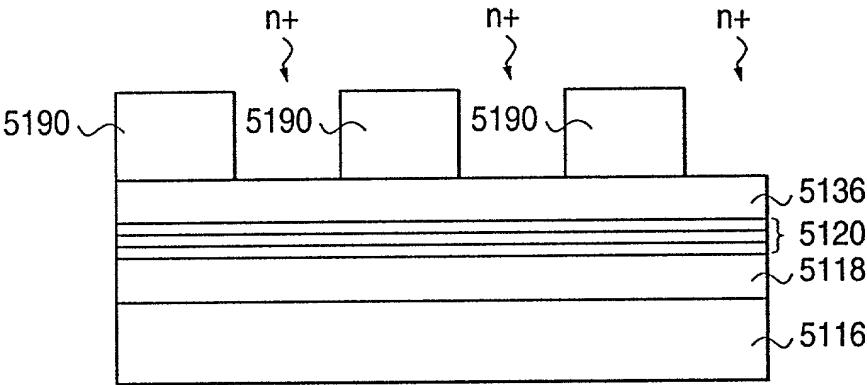


FIG. 81F

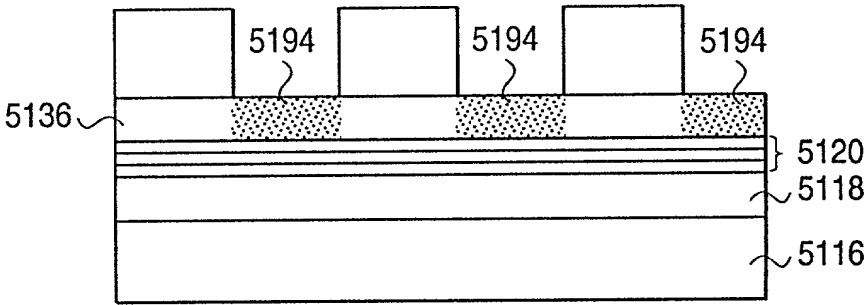


FIG. 81G

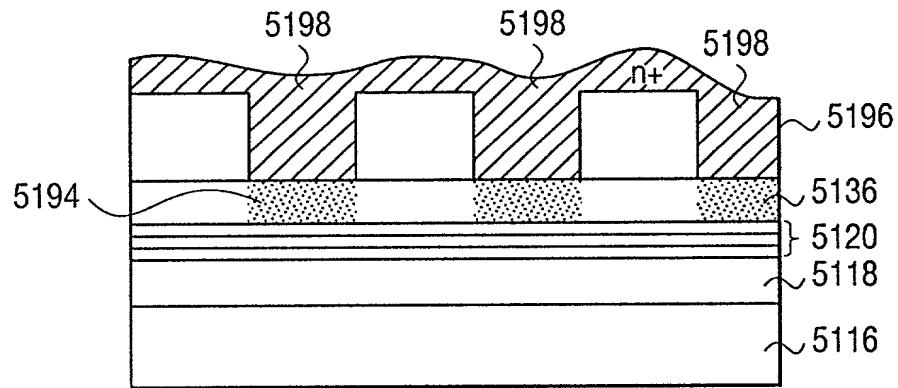


FIG. 81H

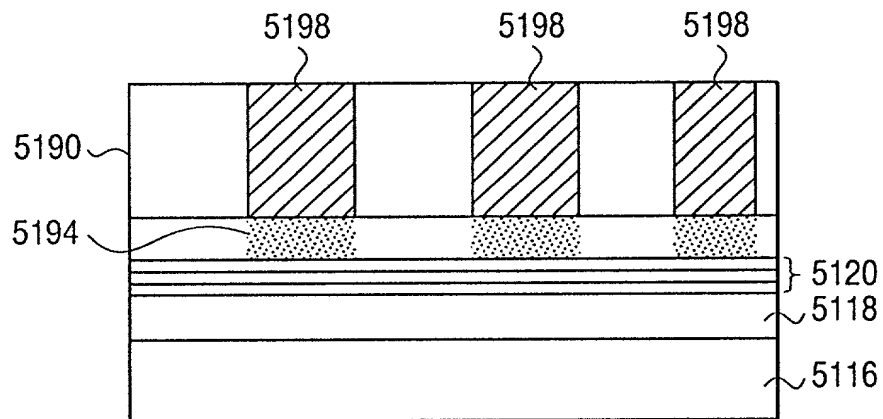


FIG. 82A

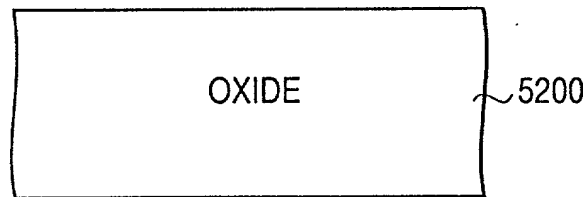


FIG. 82B

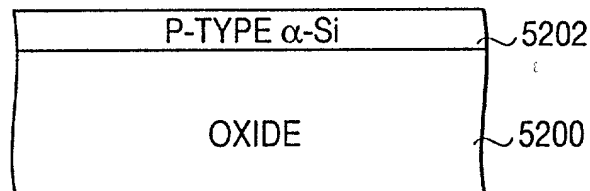


FIG. 82C

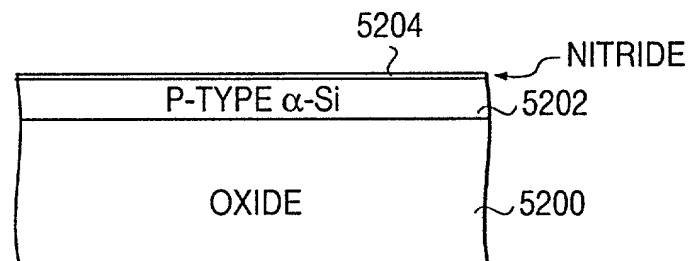


FIG. 82D

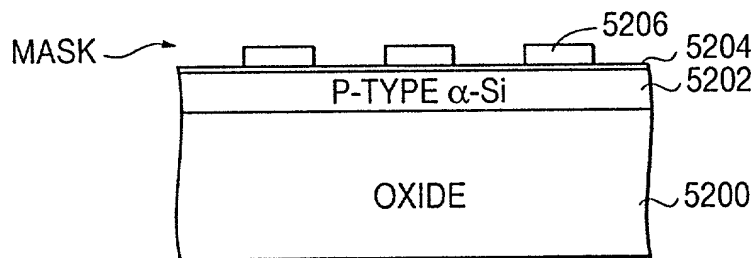


FIG. 82E

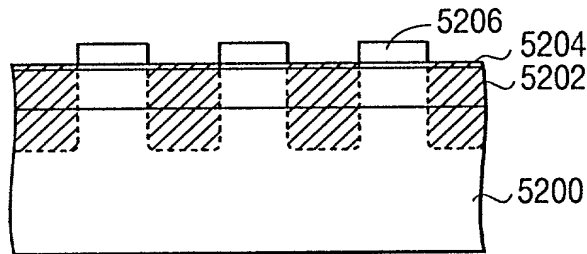


FIG. 82F

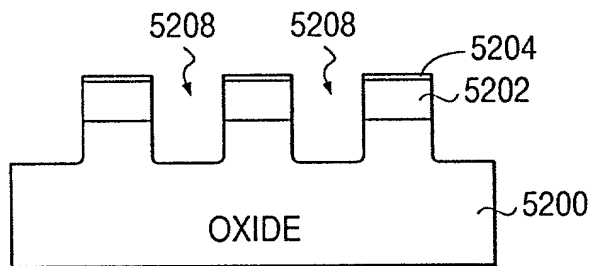


FIG. 82G

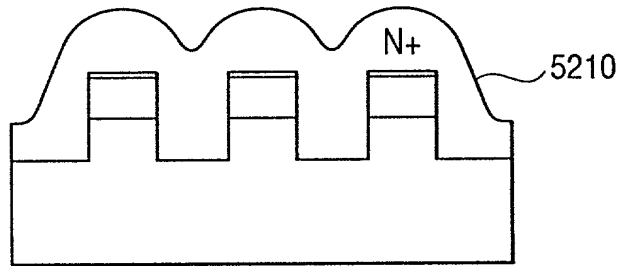


FIG. 82H

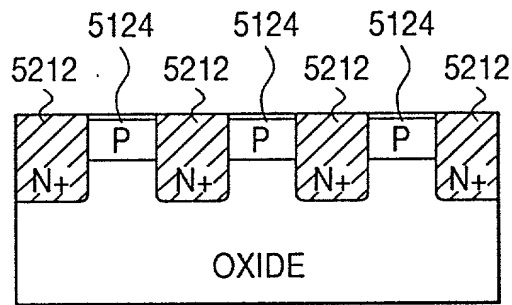


FIG. 82I

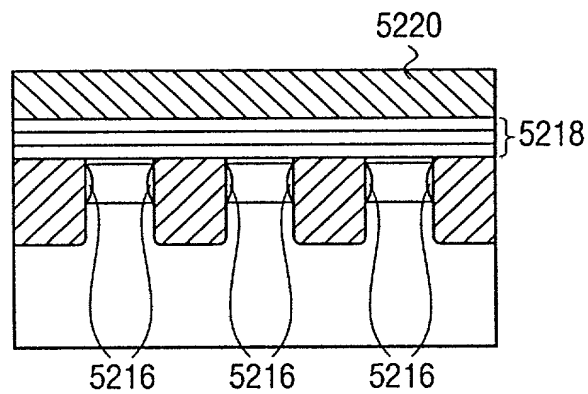


FIG. 83A

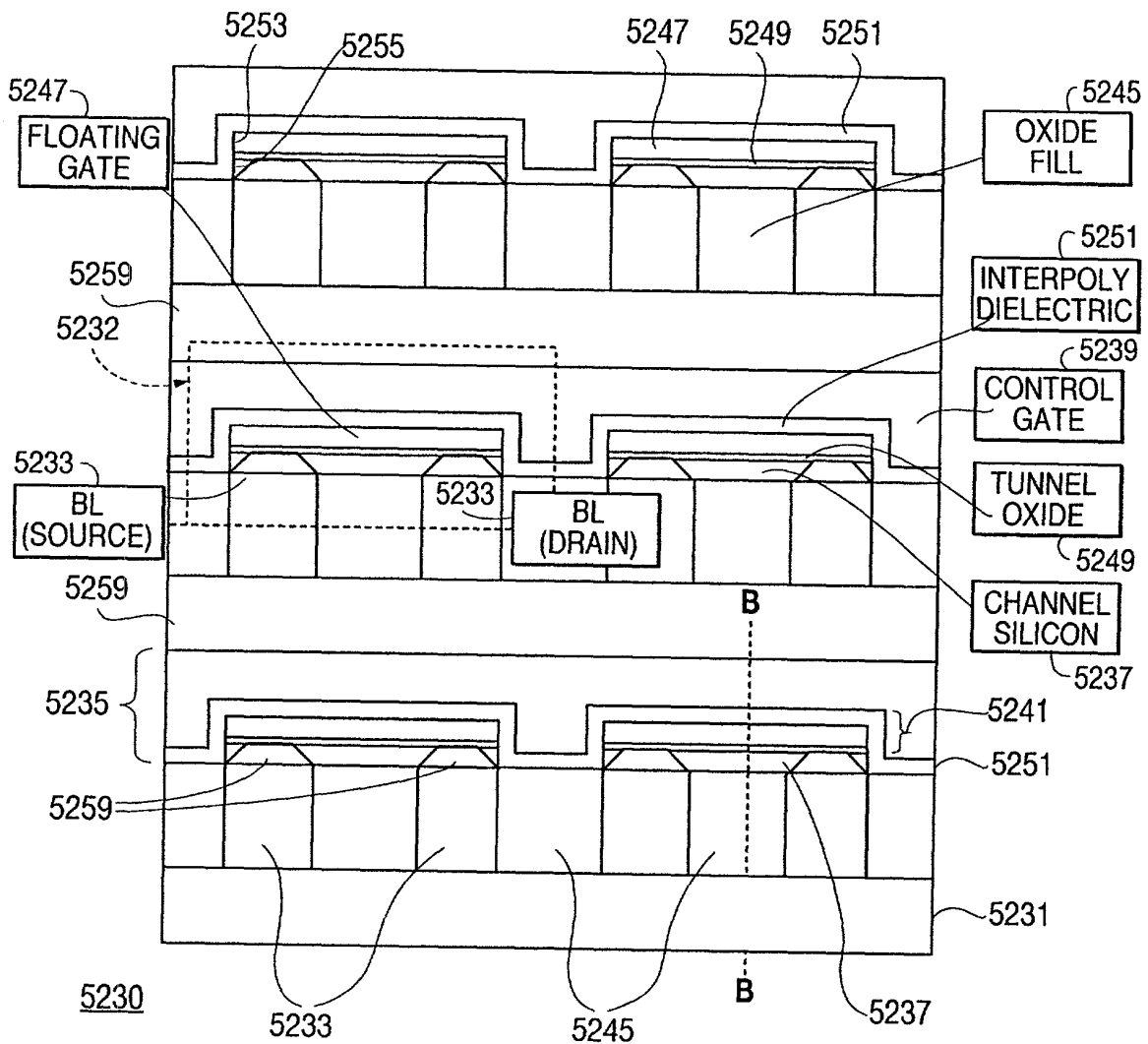


FIG. 83B

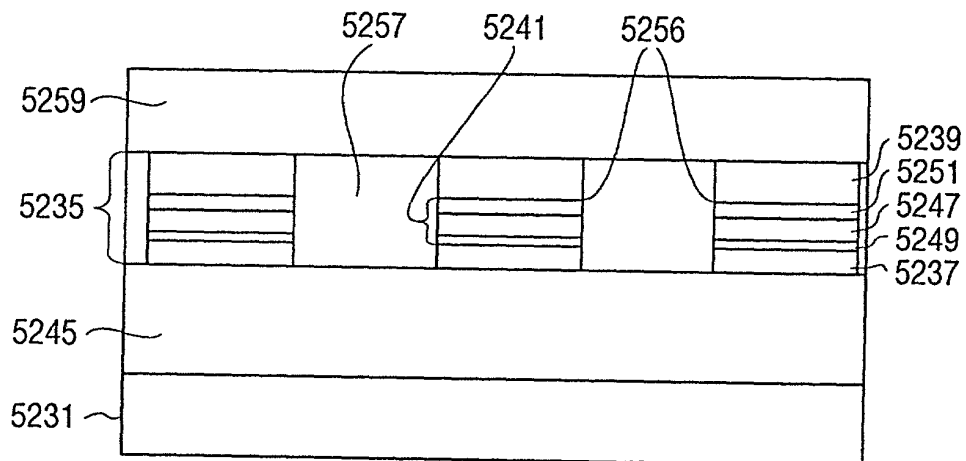


FIG. 84

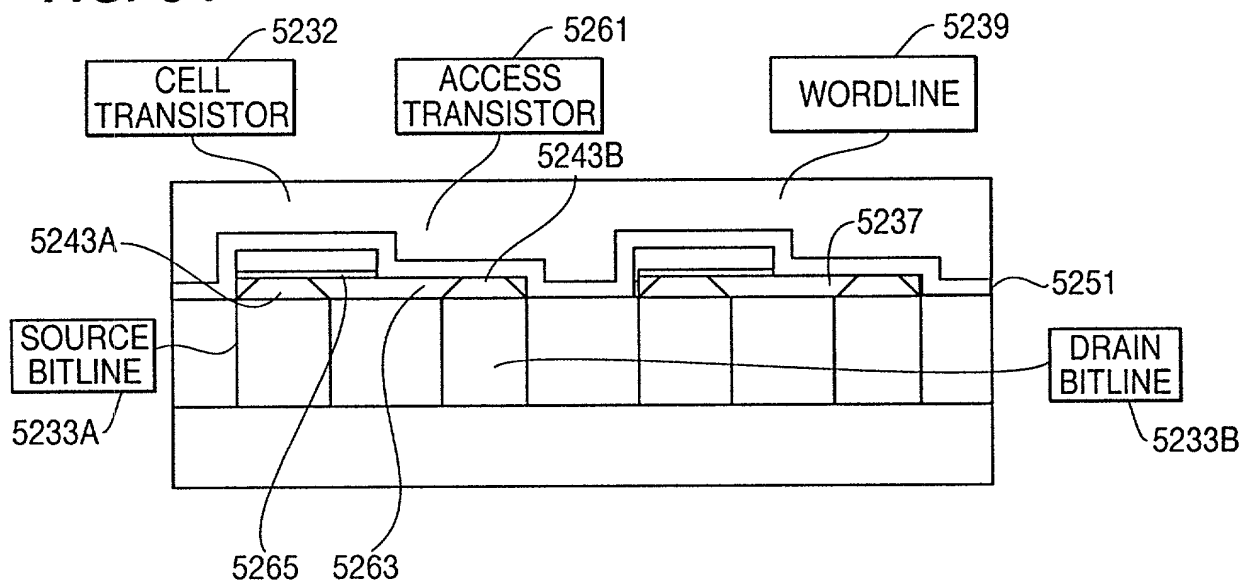


FIG. 85

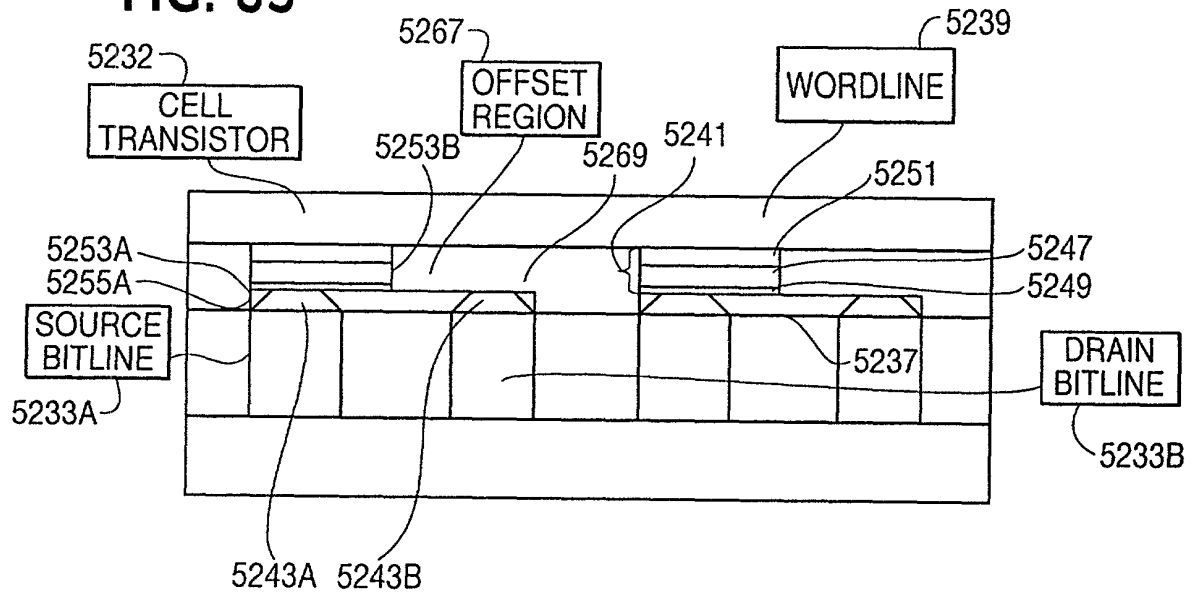


FIG. 86A

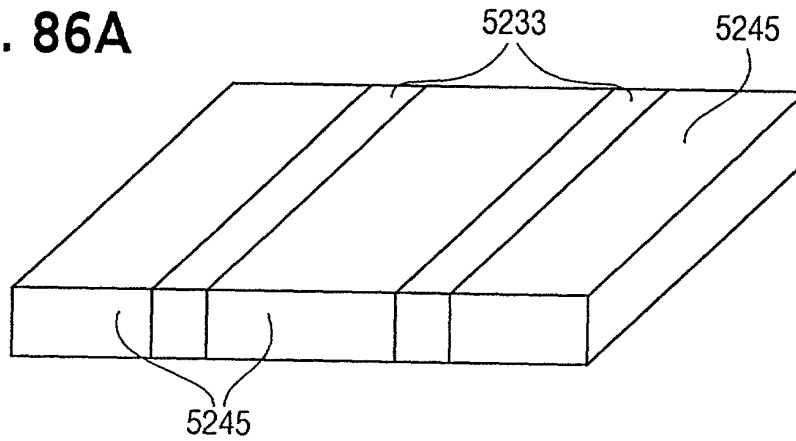


FIG. 86B

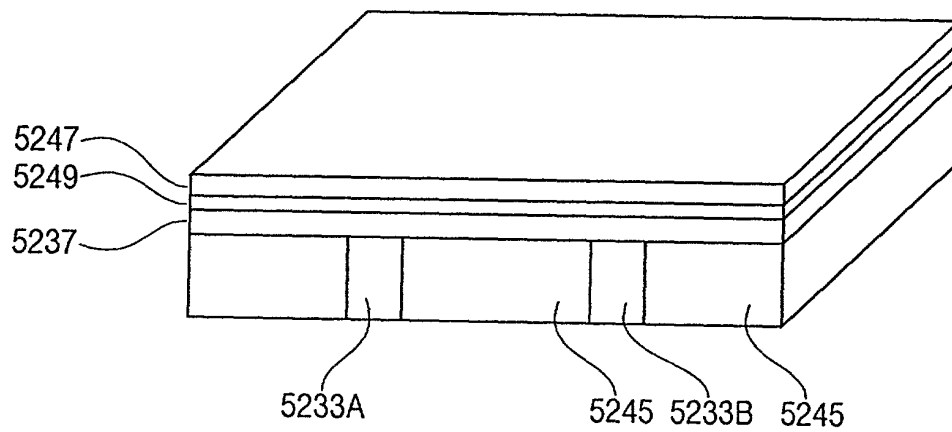


FIG. 86C

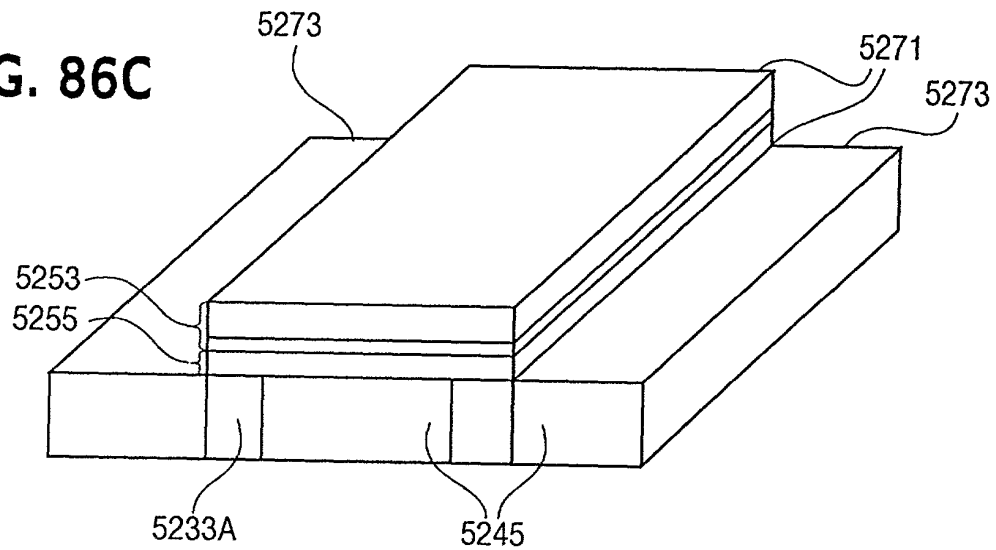


FIG. 86D

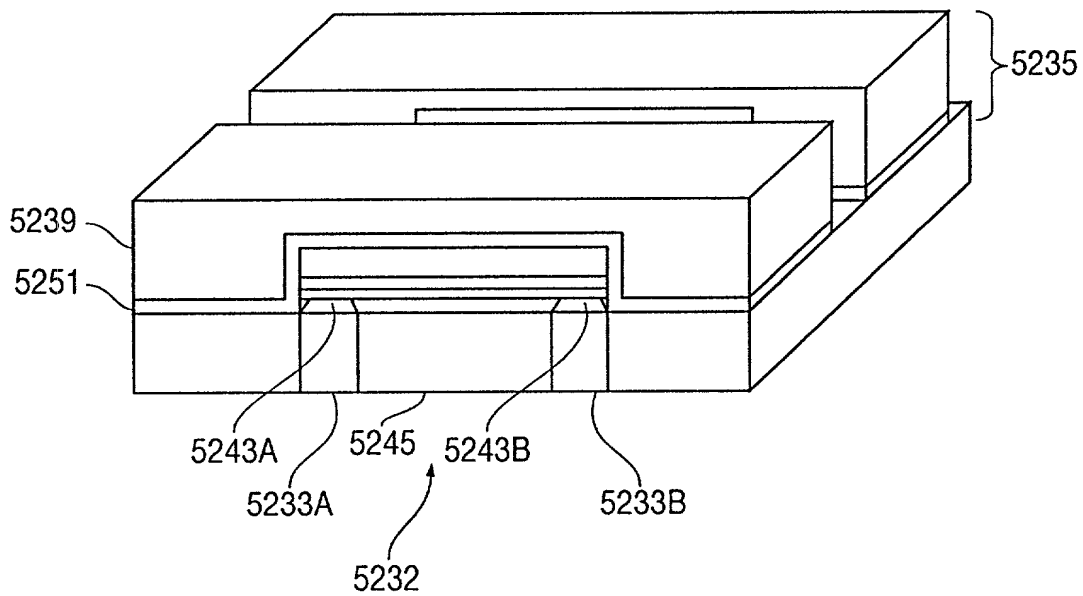


FIG. 86E

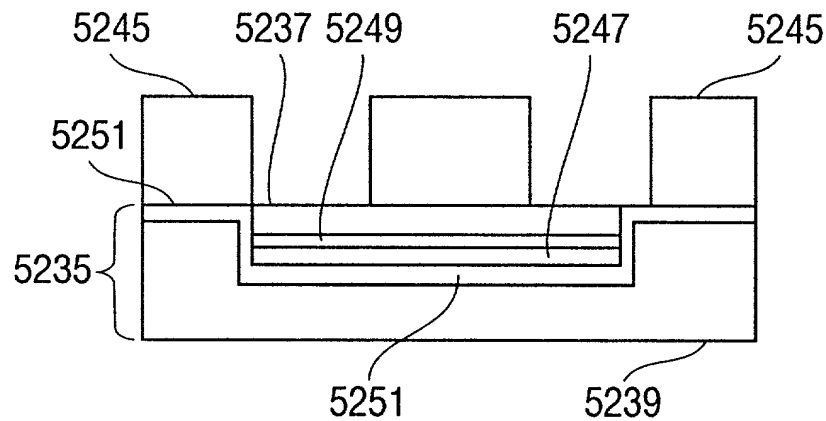


FIG. 86F

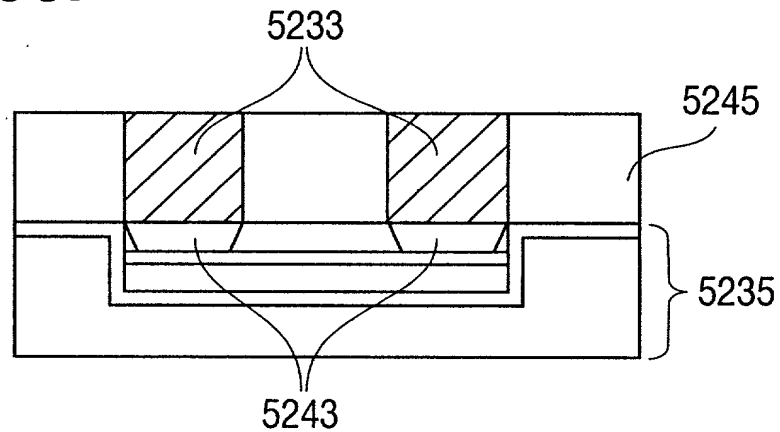


FIG. 86G

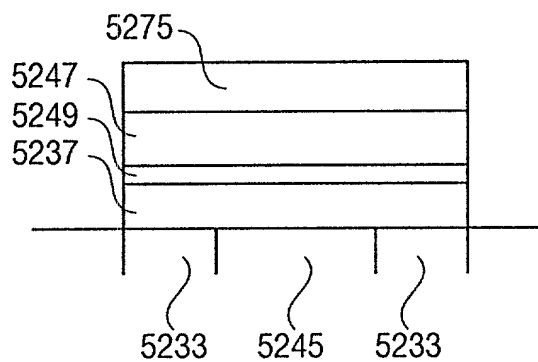


FIG. 86H

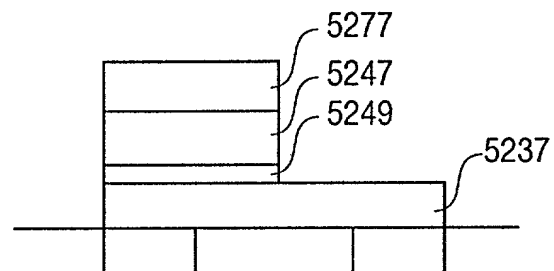


FIG. 86I

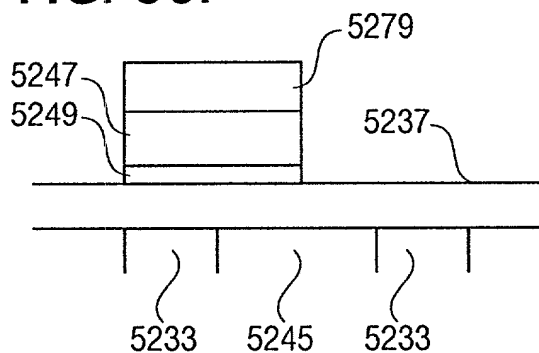


FIG. 86J

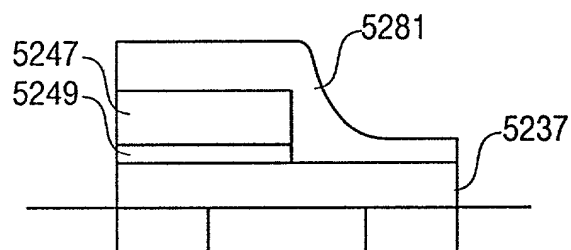


FIG. 87

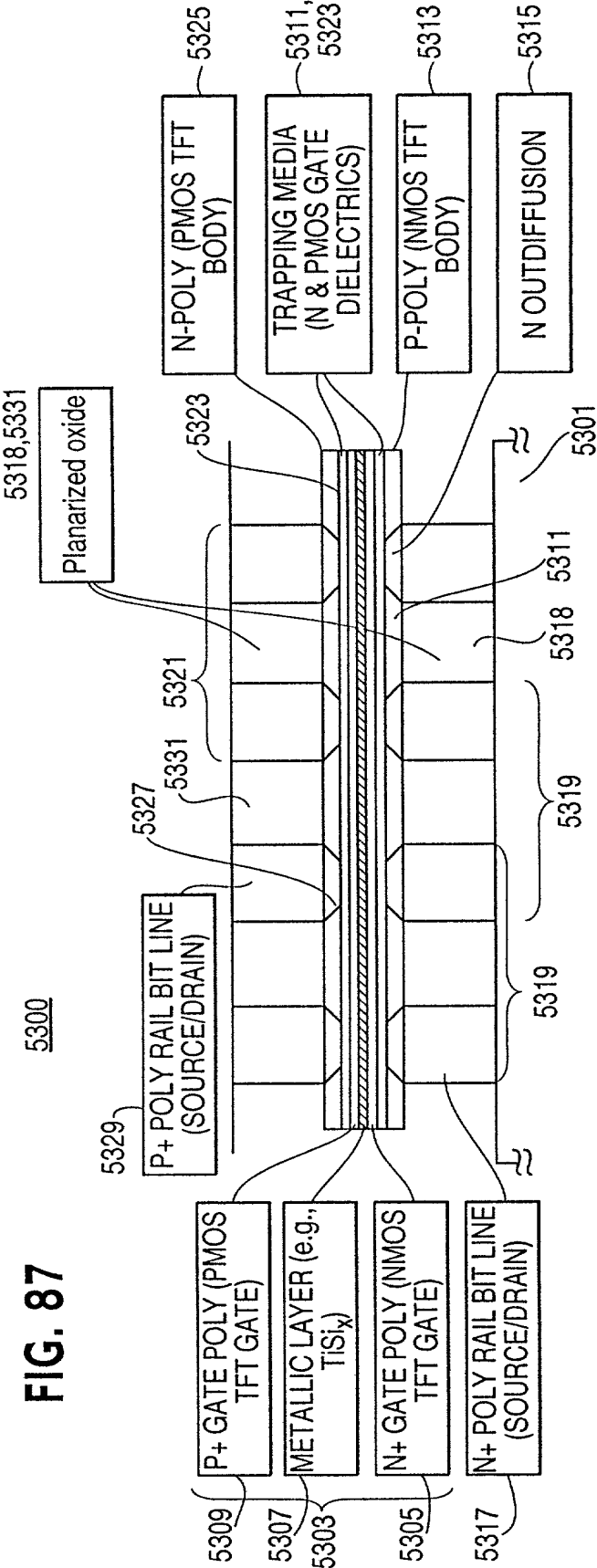


FIG. 88A

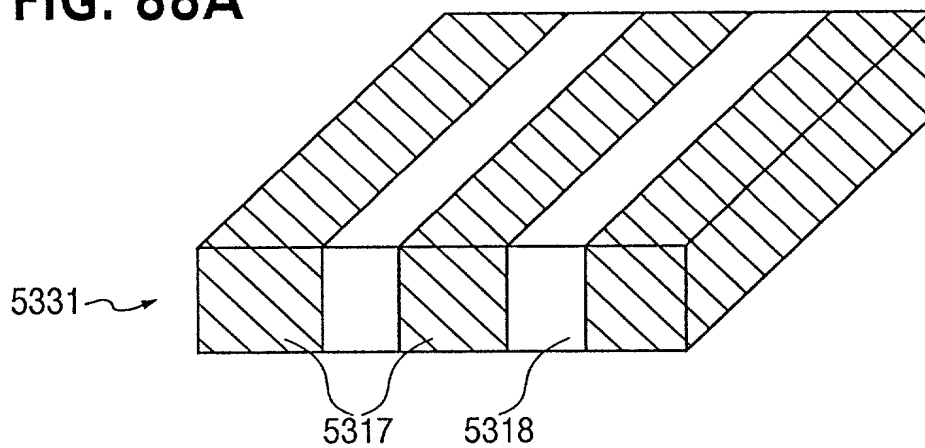


FIG. 88B

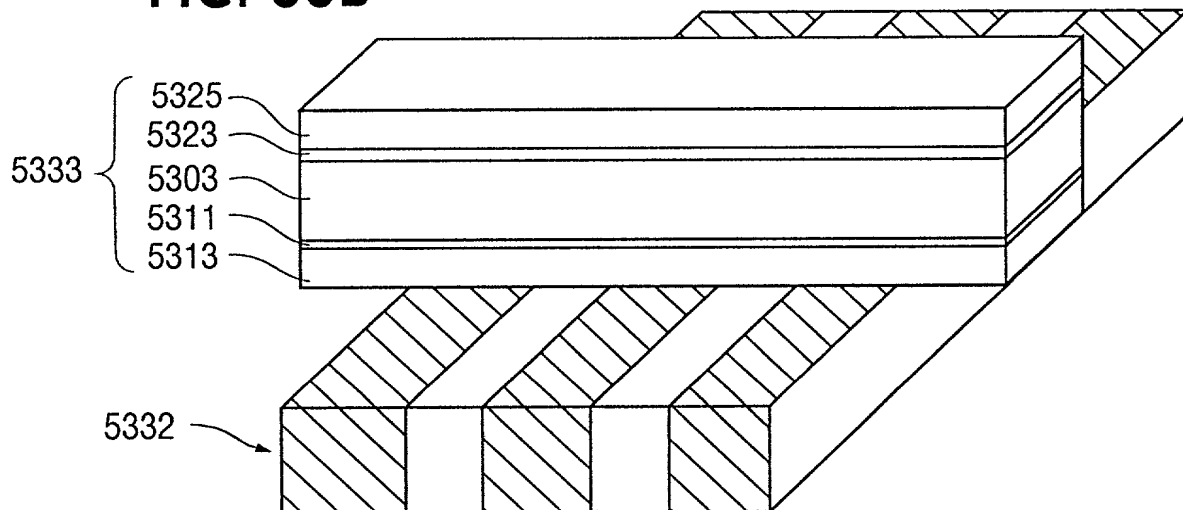


FIG. 88C

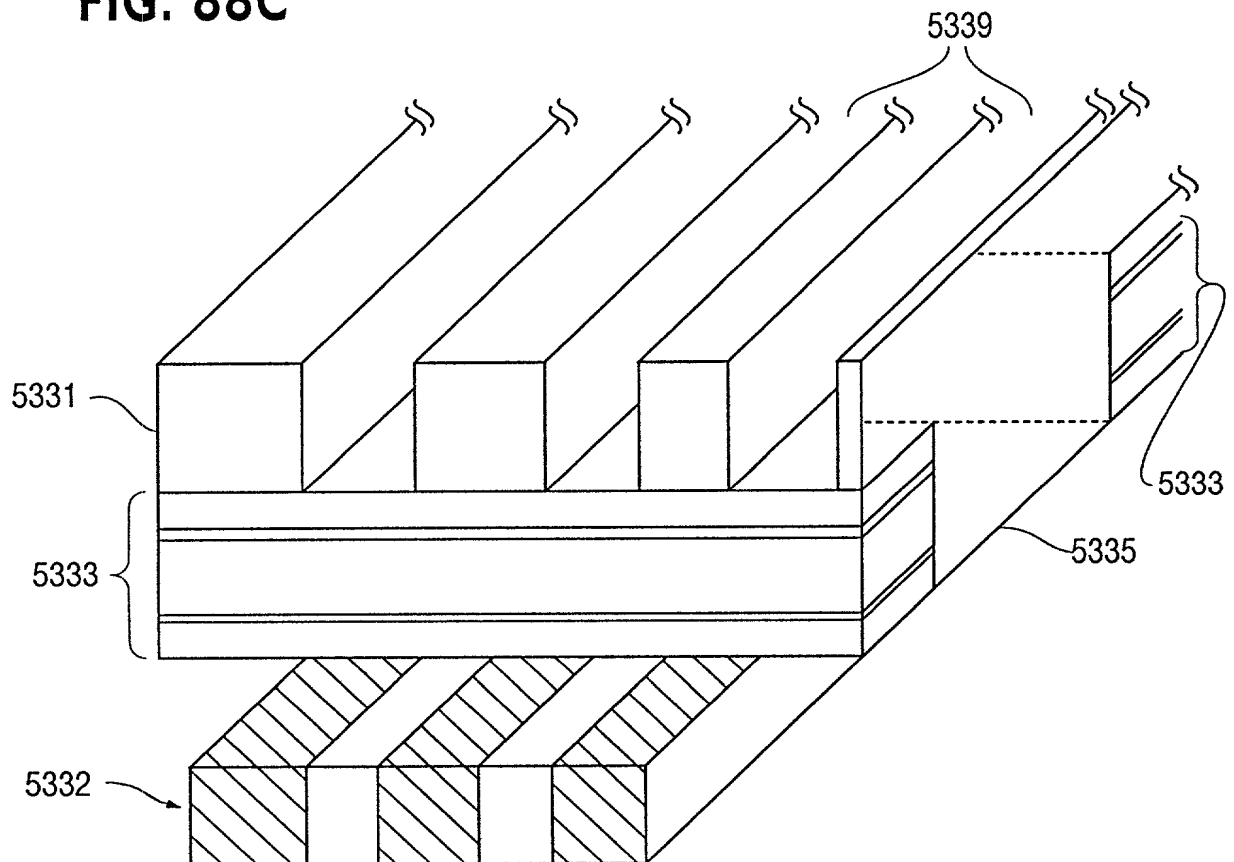


FIG. 88D

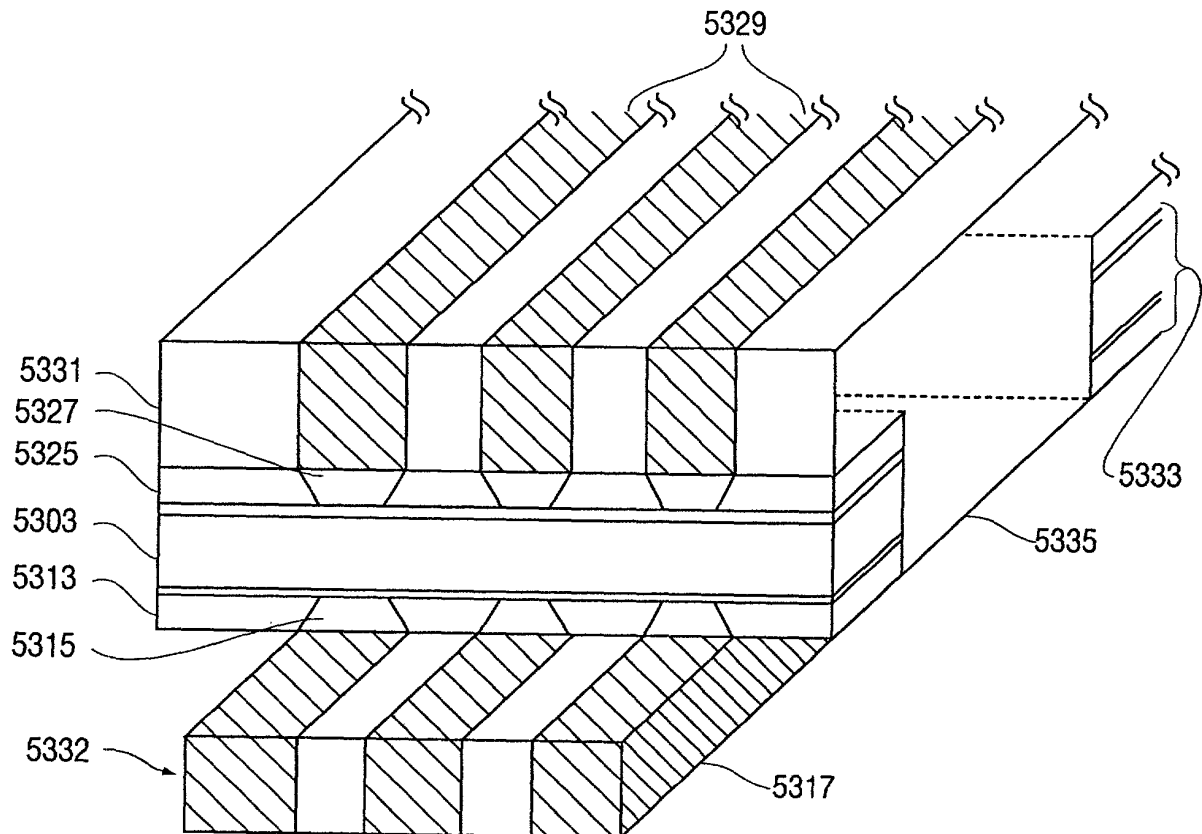


FIG. 89

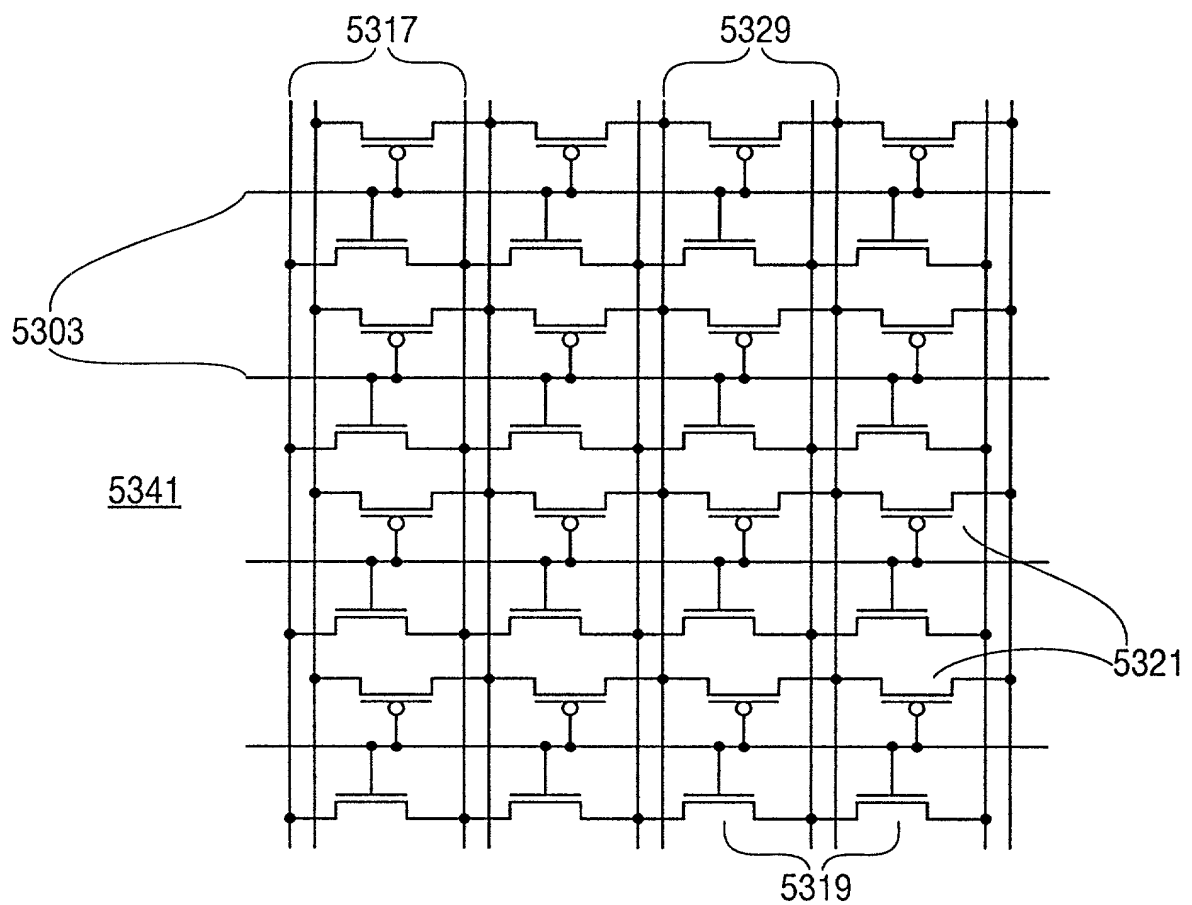


FIG. 90

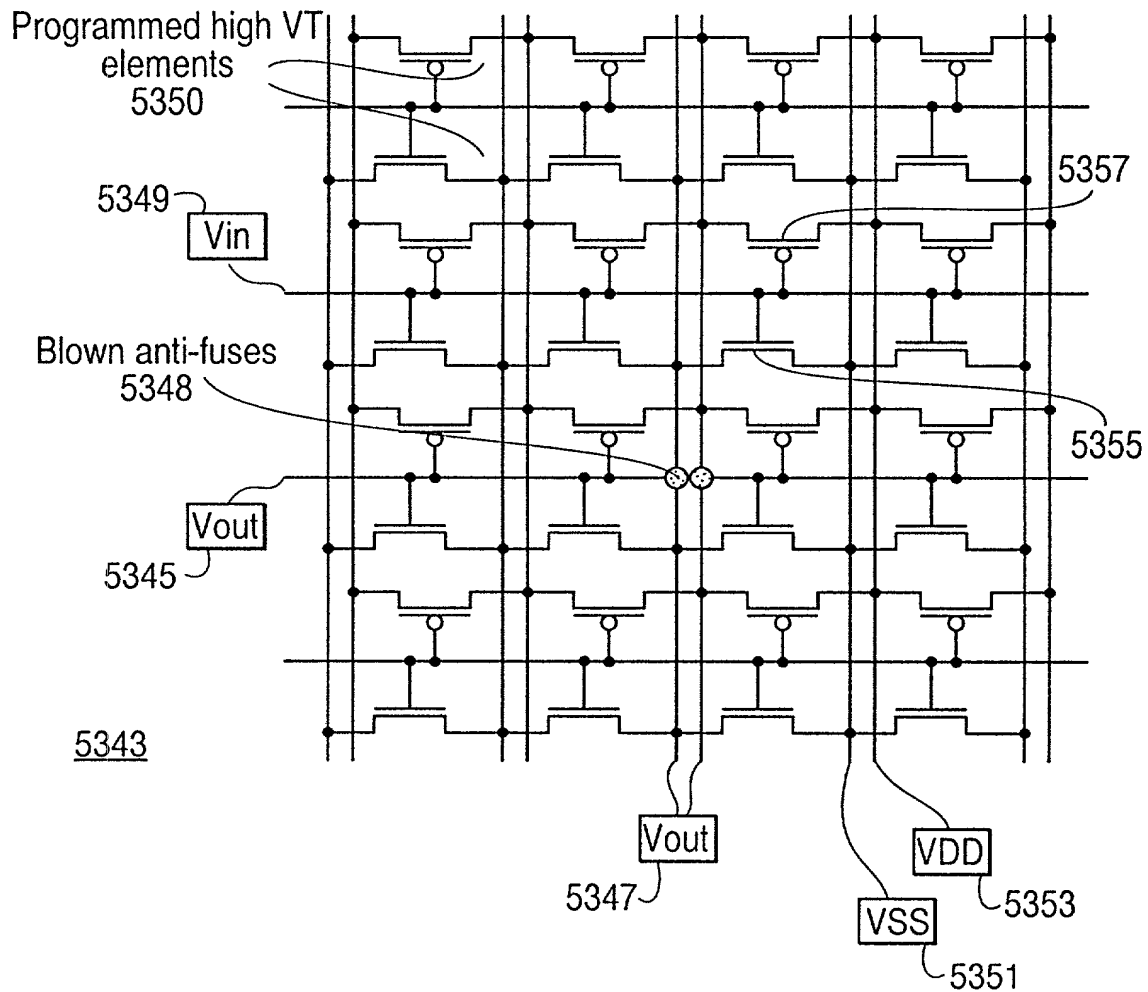


FIG. 91

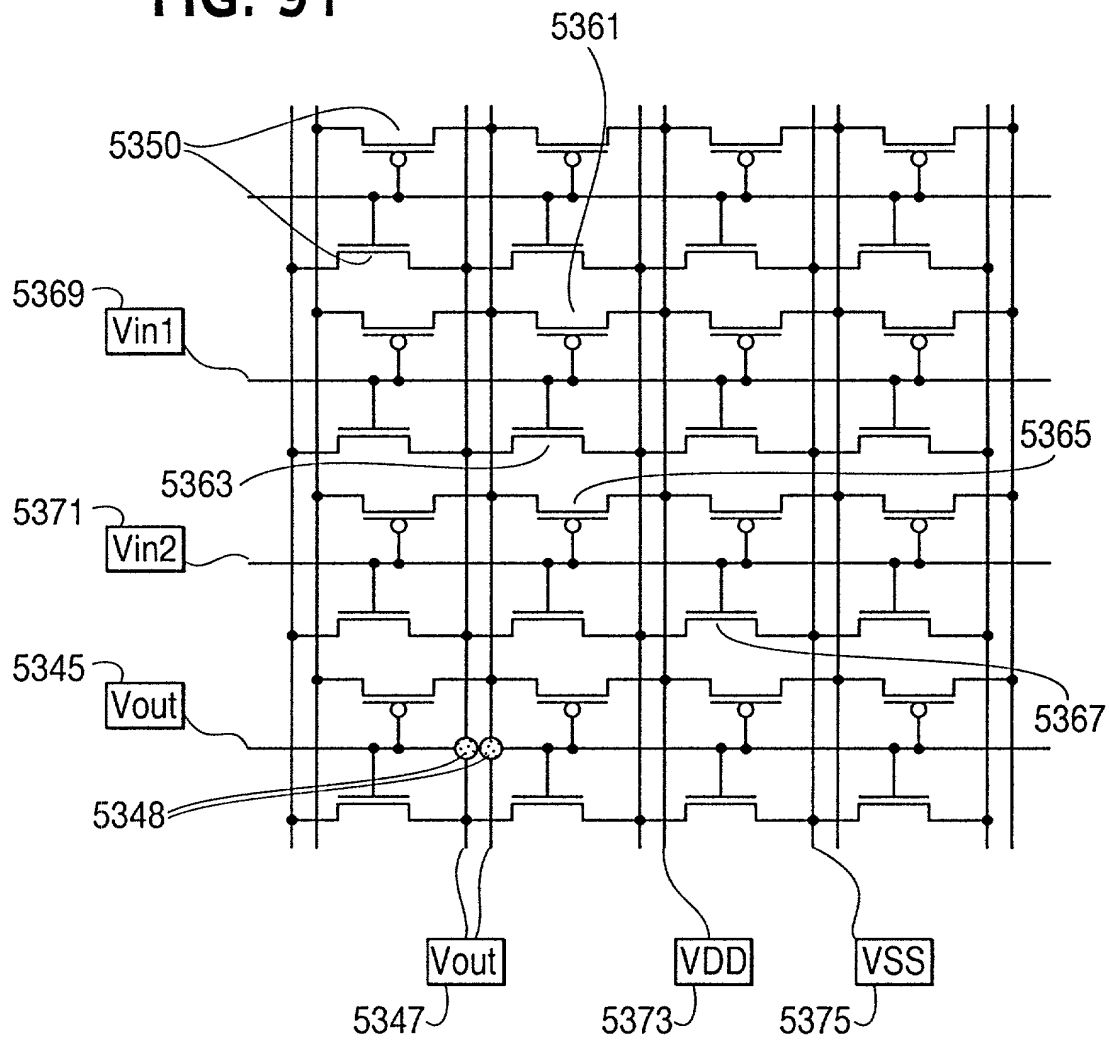


FIG. 92

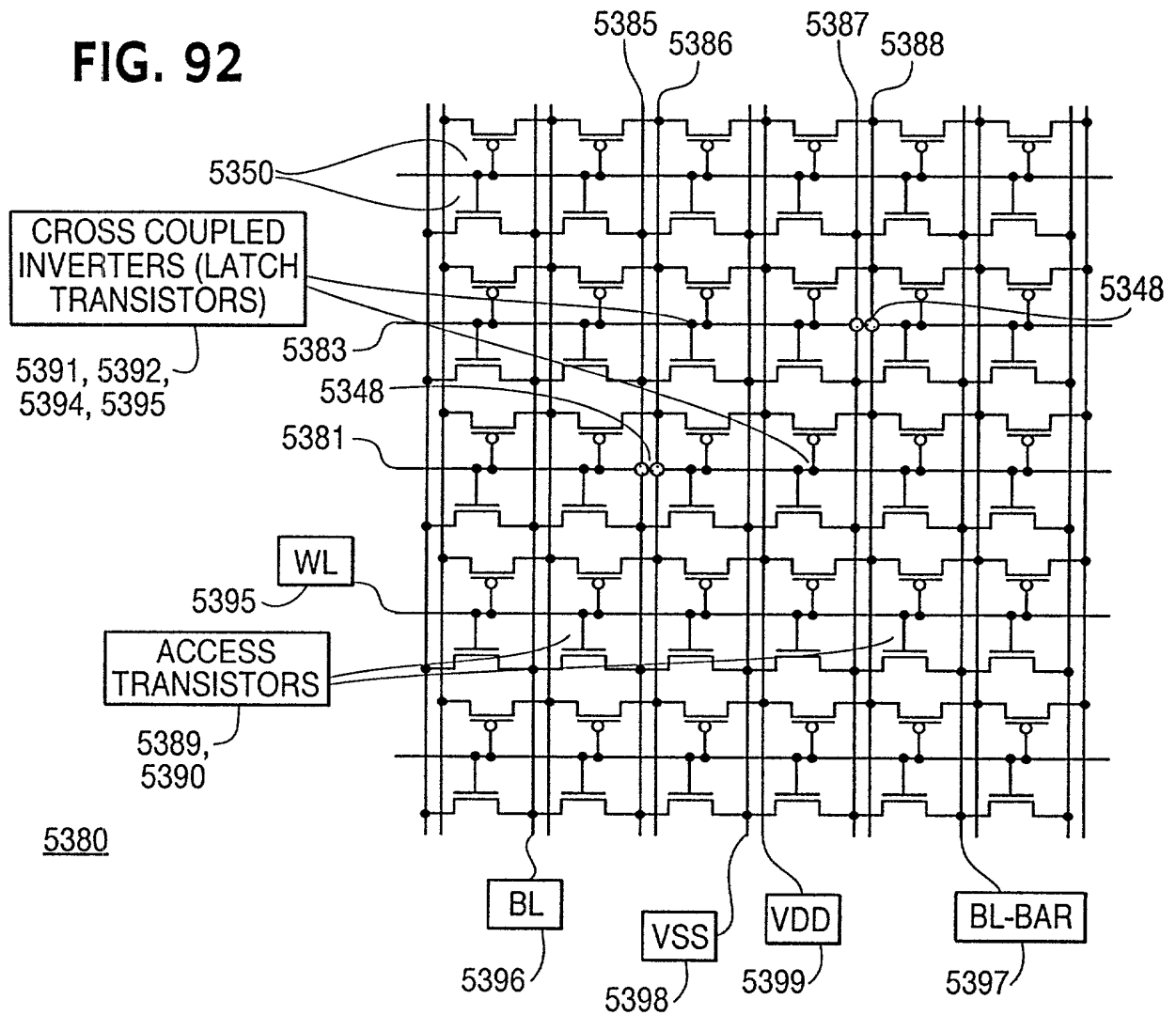


FIG. 93

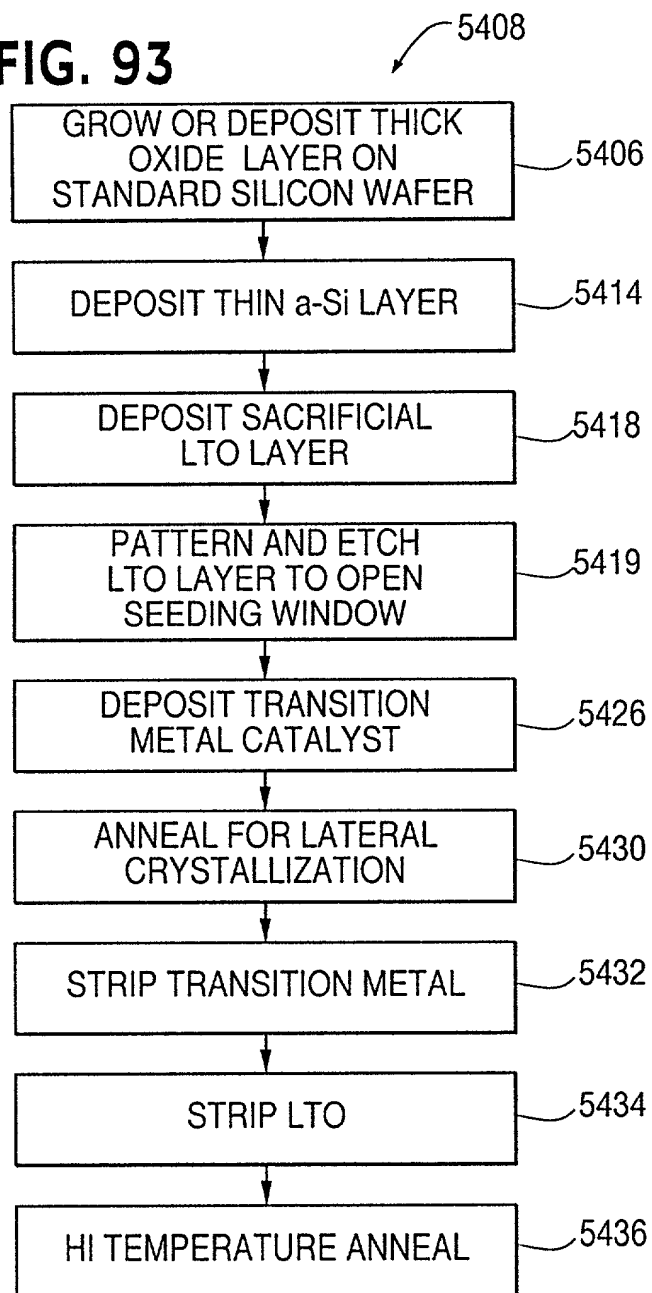


FIG. 94A

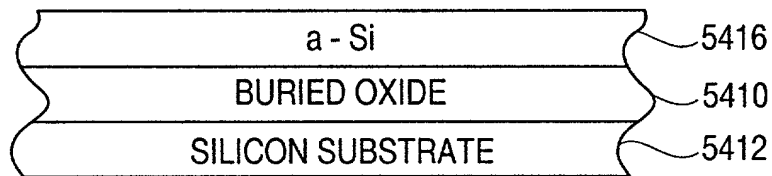


FIG. 94B

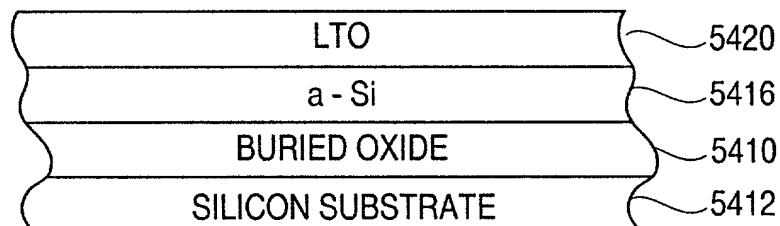


FIG. 94C

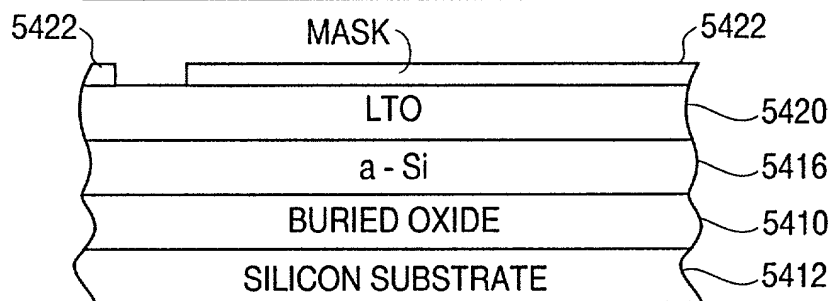


FIG. 94D

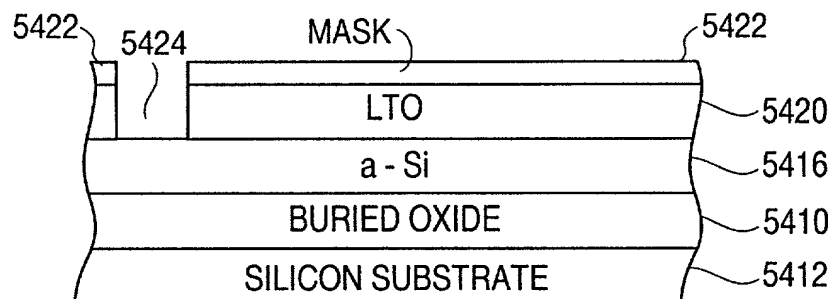


FIG. 94E

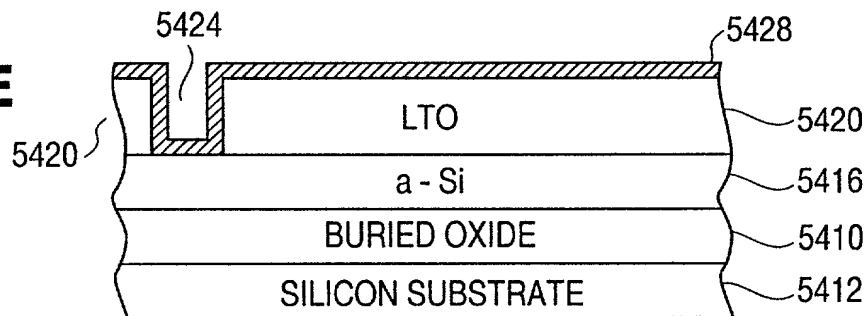


FIG. 94F

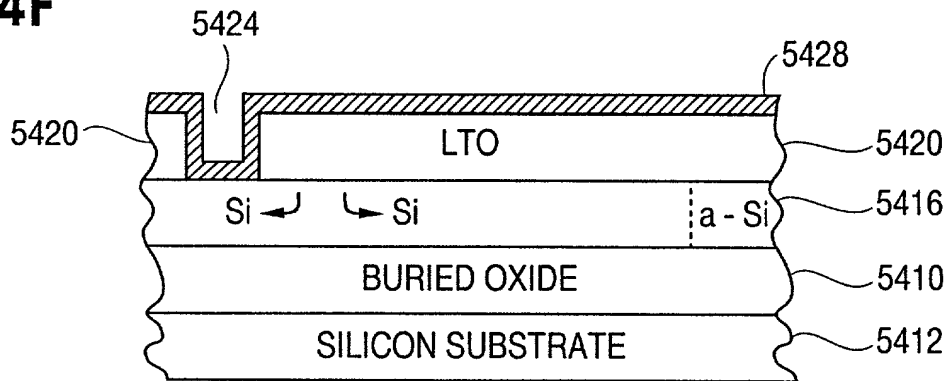


FIG. 94G

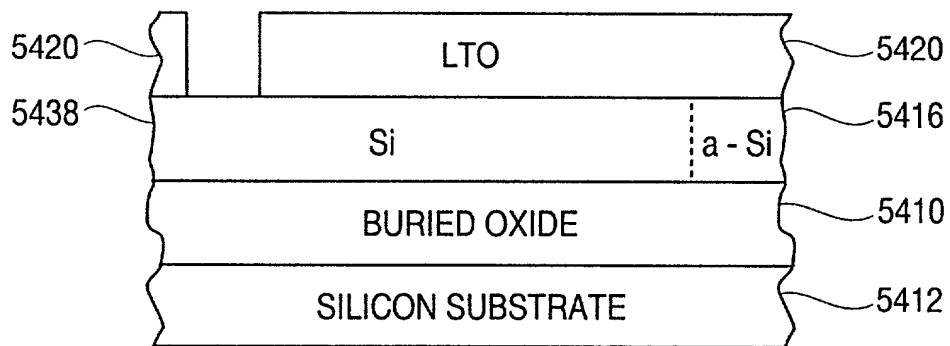


FIG. 94H

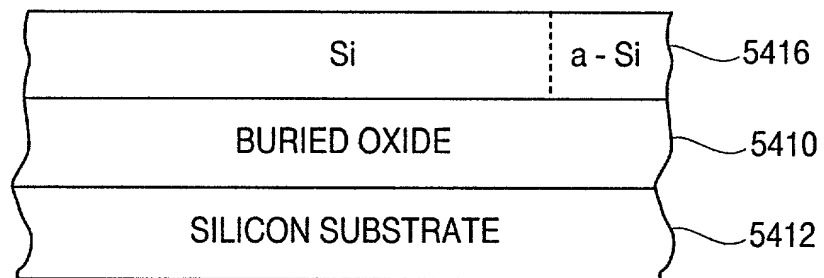
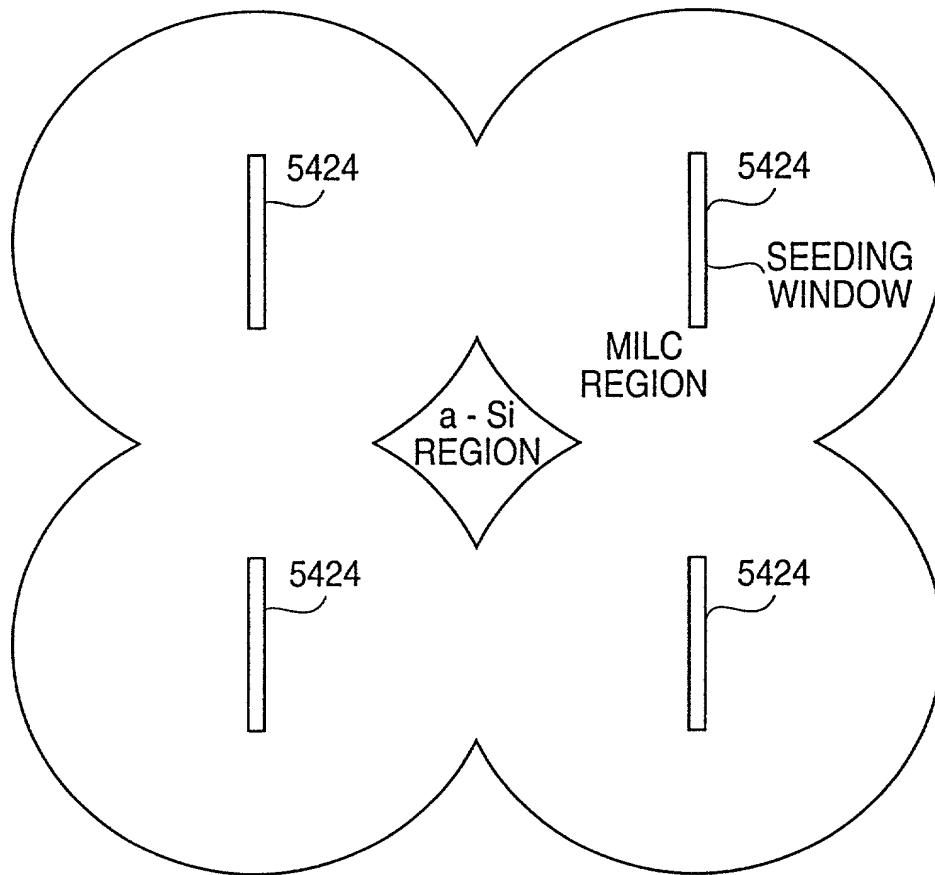


FIG. 95



09/927,648-11401

FIG. 96
(PRIOR ART)

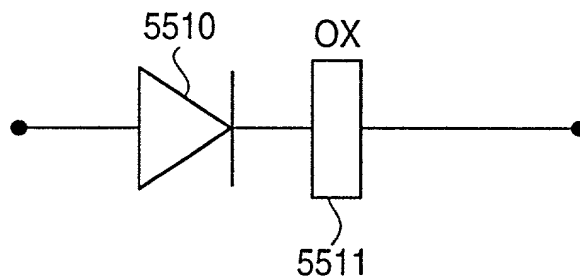


FIG. 97
(PRIOR ART)

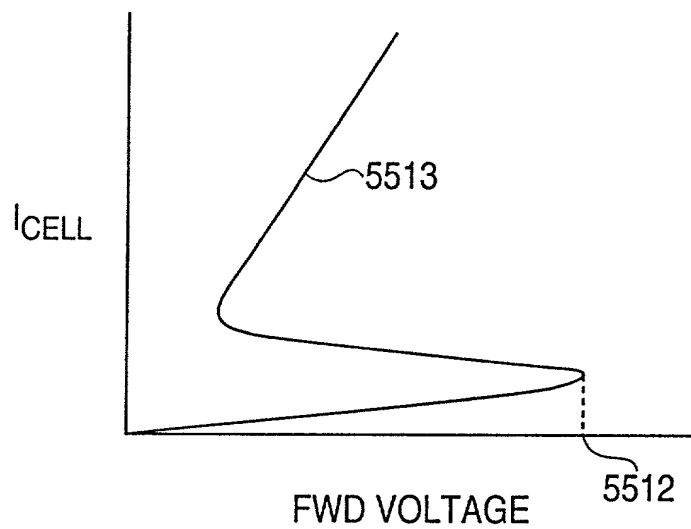


FIG. 98
(PRIOR ART)

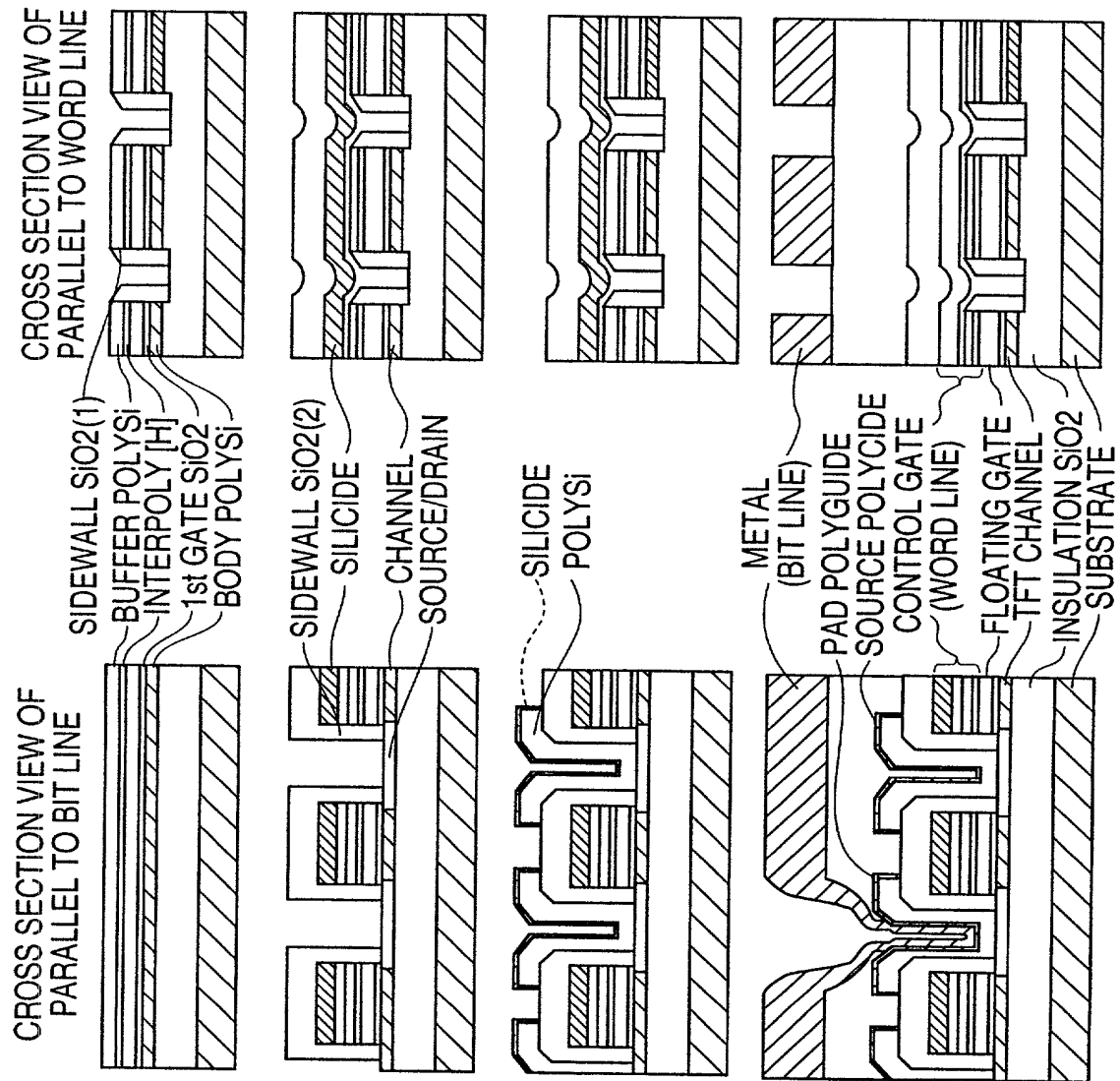


FIG. 99
(PRIOR ART)

FIG. 99 is a cross-sectional view of a semiconductor device, labeled as prior art. The device features a substrate 5610 with a series of rectangular regions 5612. Each region 5612 is covered by a layer of oxide 5614. A floating gate 5622 is positioned above the oxide layer 5614, and a control gate poly layer 5624 is positioned above the floating gate 5622. The regions 5612 are separated by gaps 5620. The floating gate 5622 and control gate poly layer 5624 are continuous across the device. The regions 5612 are labeled as N+ regions.

FIG. 100
(PRIOR ART)

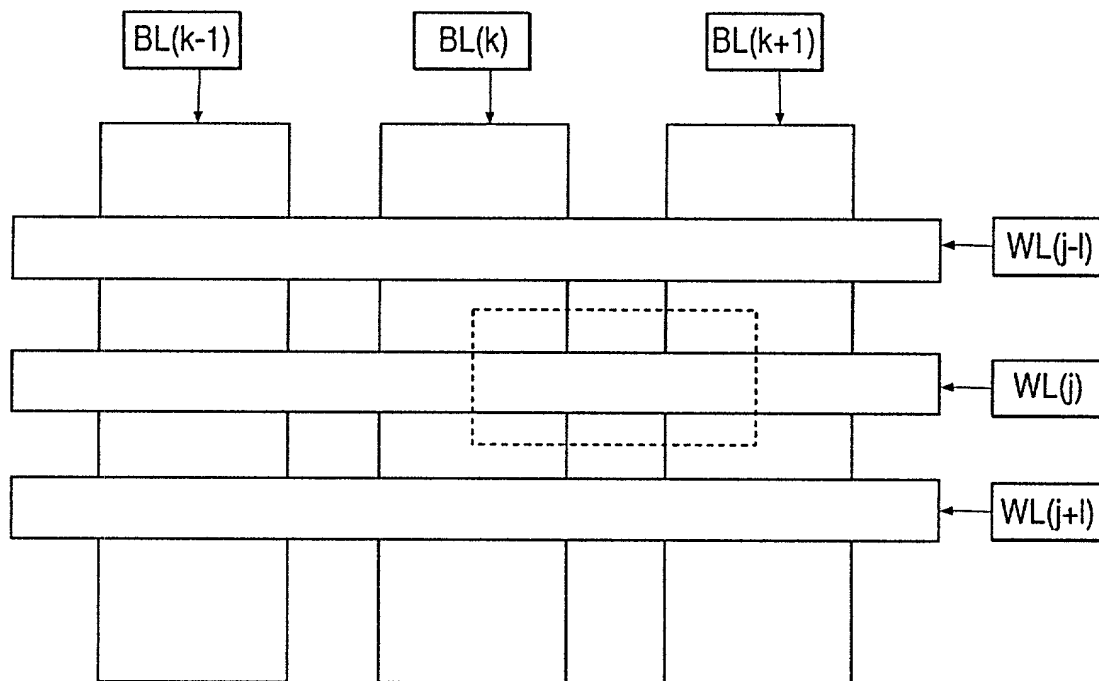


FIG. 101
(PRIOR ART)

